



Intel® PXA26x Processor Family

Design Guide — Revision 1.0

October 2002

Order Number: 278639-001



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® PXA26x Processor Family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

MPEG is an international standard for video compression/decompression promoted by ISO. Implementations of MPEG CODECs, or MPEG enabled platforms may require licenses from various entities, including Intel Corporation.

This document and the software described in it are furnished under license and may only be used or copied in accordance with the terms of the license. The information in this document is furnished for informational use only, is subject to change without notice, and should not be construed as a commitment by Intel Corporation. Intel Corporation assumes no responsibility or liability for any errors or inaccuracies that may appear in this document or any software that may be provided in association with this document. Except as permitted by such license, no part of this document may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without the express written consent of Intel Corporation.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, 2002

AlertVIEW, i960, AnyPoint, AppChoice, BoardWatch, BunnyPeople, CablePort, Celeron, Chips, Commerce Cart, CT Connect, CT Media, Dialogic, DM3, EtherExpress, ETOX, FlashFile, GatherRound, i386, i486, iCat, iCOMP, Insight960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel ChatPad, Intel Create&Share, Intel Dot.Station, Intel GigaBlade, Intel InBusiness, Intel Inside, Intel Inside logo, Intel NetBurst, Intel NetStructure, Intel Play, Intel Play logo, Intel Pocket Concert, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel TeamStation, Intel WebOutfitter, Intel Xeon, Intel XScale, Itanium, JobAnalyst, LANDesk, LanRover, MCS, MMX, MMX logo, NetPort, NetportExpress, Optimizer logo, OverDrive, Paragon, PC Dads, PC Parents, Pentium, Pentium II Xeon, Pentium III Xeon, Performance at Your Command, ProShare, RemoteExpress, Screamlane, Shiva, SmartDie, Solutions960, Sound Mark, StorageExpress, The Computer Inside, The Journey Inside, This Way In, TokenExpress, Trillium, Vivonic, and VTune are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Contents

1	Introduction	1-1
1.1	Functional Overview	1-1
1.2	Package Information	1-2
1.2.1	Package Introduction	1-2
1.2.2	Signal Pin Descriptions	1-3
2	System Memory Interface	2-1
2.1	Overview	2-1
2.1.1	Internal Flash Connections	2-3
2.2	SDRAM Interface	2-5
2.3	SDRAM memory wiring diagram	2-5
2.4	SDRAM Support	2-7
2.5	SDRAM Address Mapping	2-8
2.6	Static Memory	2-9
2.6.1	Overview	2-9
2.6.2	Boot Time Defaults	2-10
2.6.3	Flash Memory	2-10
2.6.3.1	Additional Flash Memory	2-11
2.6.3.2	Synchronous Intel StrataFlash® Memory Reset	2-11
2.6.4	SRAM / ROM / Flash / Synchronous Fast Flash Memory Options	2-11
2.6.5	Variable Latency I/O Interface Overview	2-12
2.6.6	External Logic for PCMCIA Implementation	2-14
2.6.7	DMA / Companion Chip Interface	2-17
2.7	System Memory Layout Guidelines	2-20
2.7.1	System Memory Topologies (Min and Max Simulated Loading)	2-20
2.7.2	System Memory Recommended Trace Lengths	2-21
3	LCD Display Controller	3-1
3.1	LCD Display Overview	3-1
3.2	Passive (DSTN) Displays	3-1
3.2.1	Typical Connections for Passive Panel Displays	3-2
3.2.1.1	Passive Monochrome Single Panel Displays	3-2
3.2.1.2	Passive Monochrome Single Panel Displays, Double-Pixel Data	3-3
3.2.1.3	Passive Monochrome Dual Panel Displays	3-3
3.2.1.4	Passive Color Single Panel Displays	3-4
3.2.1.5	Passive Color Dual Panel Displays	3-4
3.3	Active (TFT) Displays	3-5
3.3.1	Typical connections for Active Panel Displays	3-6
3.4	Intel® PXA26x Processor Family Pinout	3-7
3.5	Additional Design Considerations	3-8
3.5.1	Contrast Voltage	3-8
3.5.2	Backlight Inverter	3-8
3.5.3	Signal Routing and Buffering	3-8
3.5.4	Panel Connector	3-9
4	USB Interface	4-1
4.1	Self Powered Device	4-1

4.1.1	Operation if GPIO _n and GPIO _x are Different Pins	4-2
4.1.2	Operation if GPIO _n and GPIO _x are the Same Pin	4-2
4.2	Bus Powered Device	4-2
4.3	Single-Ended USB connection	4-2
5	MultiMediaCard (MMC)	5-1
5.1	Schematics	5-1
5.1.1	Signal Description	5-1
5.1.2	How to Wire	5-2
5.1.2.1	SDCard Socket	5-4
5.1.2.2	MMC Socket	5-4
5.1.3	Simplified Schematic	5-5
5.1.4	Pull-up and Pull-down	5-6
5.2	Utilized Features	5-6
6	AC97	6-1
6.1	Schematics	6-1
6.2	Layout	6-2
7	I2C	7-1
7.1	Schematics	7-1
7.1.1	Signal Description	7-1
7.1.2	Digital-to-Analog Converter (DAC)	7-2
7.1.3	Other Uses of I2C	7-2
7.1.4	Pull-Ups and Pull-Downs	7-3
7.2	Utilized Features	7-4
8	Power and Clocking	8-1
8.1	Operating Conditions	8-1
8.2	Electrical Specifications	8-1
8.3	Oscillator Electrical Specifications	8-2
8.3.1	32.768 kHz Oscillator Specifications	8-2
8.3.2	3.6864 MHz Oscillator Specifications	8-3
8.4	Reset and Power AC Timing Specifications	8-4
8.4.1	Power Supply Connectivity	8-4
8.4.2	Power On Timing	8-9
8.4.3	Hardware Reset Timing	8-10
8.4.4	Watchdog Reset Timing	8-11
8.4.5	GPIO Reset Timing	8-11
8.4.6	Sleep Mode Timing	8-11
8.5	Memory Bus and PCMCIA AC Specifications	8-12
9	JTAG/Debug Port	9-1
9.1	Description	9-1
9.2	Schematics	9-1
9.3	Layout	9-2
A	BBPXA2xx Development Baseboard Schematic Diagrams	A-1
B	PXA26x Processor Card Schematic Diagram	B-1

Figures

1-1	Processor Block Diagram	1-2
1-2	Intel® PXA26x Processor Family	1-11
2-1	General Memory Interface Configuration	2-2
2-2	PXA261 Processor Internal Configuration	2-4
2-3	PXA262 Processor Internal Configuration	2-5
2-4	SDRAM Memory System Example	2-6
2-5	Flash Memory Reset Using State Machine	2-11
2-6	Flash Memory Reset Logic if Watchdog Reset is Not Necessary	2-11
2-7	32-Bit Variable Latency I/O Read Timing (Burst-of-Four, One Wait Cycle Per Beat)	2-13
2-8	Expansion Card External Logic for a Two-Socket Configuration	2-15
2-9	Expansion Card External Logic for a One-Socket Configuration	2-16
2-10	Alternate Bus Master Mode	2-18
2-11	Variable Latency I/O	2-19
2-12	CS, CKE, DQM, CLK, MA Minimum Loading Topology	2-20
2-13	CS, CKE, DQM, CLK, MA Maximum Loading Topology	2-20
2-14	MD Minimum Loading Topology	2-20
2-15	MD maximum Loading Topology	2-21
3-1	Single Panel Monochrome Passive Display Typical Connection	3-3
3-2	Passive Monochrome Single Panel Displays, Double-Pixel Data Typical Connection	3-3
3-3	Passive Monochrome Dual Panel Displays Typical Connection	3-4
3-4	Passive Color Single Panel Displays Typical Connection	3-4
3-5	Passive Color Dual Panel Displays Typical Connection	3-5
3-6	Active Color Display Typical Connection	3-7
4-1	Self Powered Device	4-1
4-2	Single-Ended USB connection	4-3
5-1	Processor MMC and SDCard Signal Connections	5-3
5-2	Processor MMC to SDCard Simplified Signal Connection	5-5
6-1	AC97 connection	6-1
7-1	Linear Technology DAC with I2C Interface	7-2
7-2	Using an Analog Switch to Allow a Second CF Card	7-3
7-3	I ² C Pull-Ups and Pull-Downs	7-3
8-1	Power-On Reset Timing	8-9
8-2	Hardware Reset Timing	8-10
8-3	GPIO Reset Timing	8-11
8-4	Sleep Mode Timing	8-12
9-1	JTAG/Debug Port Wiring Diagram	9-1

Tables

1-1	Related Documentation	1-1
1-2	Signal Pin Descriptions	1-3
1-3	Intel® PXA26x Processor Family Pin Out - Ballpad Number Order	1-12
2-1	Memory Address Map	2-3
2-2	SDRAM Memory Types Supported by the Processor	2-7
2-3	Normal Mode Memory Address Mapping	2-8
2-4	Processor Compatibility Mode Address Line Mapping	2-9
2-5	Valid Booting Configurations Based on Package Type	2-10

2-6	BOOT_SEL Definitions	2-10
2-7	SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications.....	2-12
2-8	Variable Latency I/O Interface AC Specifications	2-13
2-9	Card Interface (PCMCIA or Compact Flash) AC Specifications	2-16
2-10	Minimum and Maximum Trace Lengths for the SDRAM Signals	2-21
3-1	LCD Controller Data Pin Utilization	3-1
3-2	Passive Display Pins Required	3-2
3-3	Active Display Pins Required	3-6
3-4	Intel® PXA26x Processor Family LCD Controller Ball Positions.....	3-7
5-1	MMC Signal Description.....	5-1
5-2	SDCard Socket Signals.....	5-2
5-3	MMC Controller Supported Sockets and Devices.....	5-2
5-4	SDCard Pull-up and Pull-down Resistors	5-6
5-5	MMC Pull-up and Pull-down Resistors.....	5-6
7-1	I2C Signal Description.....	7-1
8-1	Voltage, Temperature, and Frequency Electrical Specifications.....	8-1
8-2	Absolute Maximum Ratings	8-2
8-3	32.768 kHz Oscillator Specifications.....	8-2
8-4	3.6864 MHz Oscillator Specifications.....	8-3
8-5	Intel® PXA26x Processor Family VCCN vs. VCCQ.....	8-4
8-6	Power-On Timing Specifications	8-10
8-7	Hardware Reset Timing Specifications	8-10
8-8	GPIO Reset Timing Specifications	8-11
8-9	Sleep Mode Timing Specifications	8-12
8-10	SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications.....	8-13
8-11	Variable Latency I/O Interface AC Specifications	8-13
8-12	Card Interface (PCMCIA or Compact Flash) AC Specifications	8-14
8-13	Synchronous Memory Interface AC Specifications	8-14

Revision History

Date	Revision	Description
July 2002	0.9	Initial Release: Intel® PXA26x Processor Family Design Guide
October 2002	1.0	Public Release of Intel® PXA26x Processor Family Design Guide

This document presents design recommendations, board schematics, and debug recommendations for the Intel® PXA26x Processor Family. The PXA26x processor family is a 32-bit, multi-chip device which combines a processor based on Intel® XScale™ microarchitecture and Intel StrataFlash® Memory. This document refers to all versions as the processor.

The PXA26x processor family is available in a 13x13mm 294-pin TF-BGA package. It is available in multiple versions with different flash configurations:

- PXA261 processor – 128 megabit x 16 Intel StrataFlash® Memory
- PXA262 processor – 256 megabit x 16 Intel StrataFlash® Memory

The guidelines presented in this document ensure maximum flexibility for board designers, while reducing the risk of board-related issues.

You should consult the debug recommendations in Chapter 9, “JTAG/Debug Port” and understand them when debugging a PXA26x processor family-based system to ensure the correct implementation of the debug port.

Table 1-1. Related Documentation

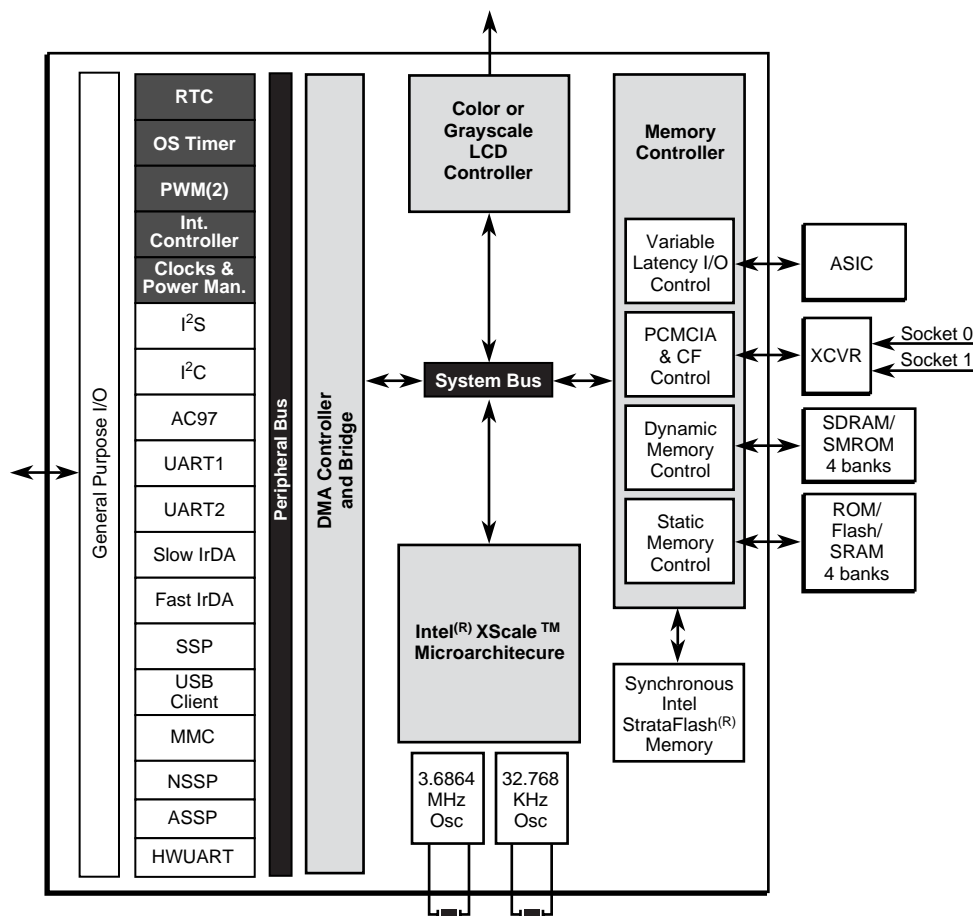
Document Title	Order Number
<i>Intel® PXA26x Processor Family Developer's Manual</i>	278638
<i>Intel® PXA26x Processor Family Electrical, Mechanical, and Thermal Specification</i>	TBD

1.1 Functional Overview

The PXA26x processor family is a multi-chip product consisting of a processor plus up to 256 Mb of Intel StrataFlash® memory. The processor integrates the Intel® XScale™ microarchitecture core with many peripherals to let you design products for the handheld market, while the Intel StrataFlash® memory combines multi-bit-per-cell technology with synchronous burst capability. Both the processor and the flash memory are contained within one 13x13mm package with a 32-bit external data bus.

Figure 1-1 is a block diagram of the processor.

Figure 1-1. Processor Block Diagram



1.2 Package Information

This section describes the package, pinout, and signal descriptions.

1.2.1 Package Introduction

Package features of the PXA26x processor family are:

- Core frequencies supported
 - 200 MHz for the PXA261 processor
 - 200 - 300 MHz for the PXA262 processor
- System memory interface
 - 100 MHz SDRAM

- 4 MB to 256 MB of SDRAM memory
- Support for 16, 64, 128, or 256 Mbit DRAM technologies
- 4 Banks of SDRAM, each supporting 64 MB of memory
- Clock enable (CKE) – provides 1 CKE pin to put the entire SDRAM interface into self refresh
- Supports as many as 5 external static memory devices (SRAM, flash, or VLIO) and 1 internal flash device
- PCMCIA/Compact Flash card control pins
- LCD Controller pins
- Full-function UART
- Bluetooth UART
- Hardware UART
- MMC Controller pins
- SSP pins
- Network SSP
- Audio SSP
- USB Client pins
- AC'97 Controller pins
- Standard UART pins
- I²C Controller pins
- PWM pins
- 20 dedicated GPIOs pins
- Integrated JTAG support
- Single-Ended USB client

1.2.2 Signal Pin Descriptions

Table 1-2 defines the signal descriptions for the processor.

Table 1-2. Signal Pin Descriptions (Sheet 1 of 8)

Name	Type	Description
Memory Controller Pins		
MA[25:0]	OCZ	Memory address bus – This bus signals the address requested for memory accesses.
MD[31:0]	ICOCZ	Memory data bus – D[31:0]: These signals are the memory data bus bits.
nOE	OCZ	Memory output enable – Connect this signal to the output enables of memory devices to control their data bus drivers.
nWE	OCZ	Memory write enable – Connect this signal to the write enables of memory devices.

Table 1-2. Signal Pin Descriptions (Sheet 2 of 8)

Name	Type	Description
nSDCS[0]	OCZ	SDRAM CS for banks 0 through 3 – Connect these signals to the chip select (CS) pins for SDRAM. nSDCS0 is a three-state signal, while nSDCS1-3 are not three-state.
nSDCS[1]	OC	
nSDCS[2]/GPIO[86]	ICOC	
nSDCS[3]/GPIO[87]	ICOC	
DQM[3:0]	OCZ	SDRAM DQM for data bytes 0 through 3 – Connect these signals to the data output mask enables (DQM) for SDRAM.
nSDRAS	OCZ	SDRAM RAS – Connect this signal to the row address strobe (RAS) pins for all banks of SDRAM.
nSDCAS	OCZ	SDRAM CAS – Connect this signal to the column address strobe (CAS) pins for all banks of SDRAM.
SDCKE[0]	OC	SDRAM or Synchronous Static Memory clock enable. ConnectSDCKE[0] to the CKE pins of SMROM. The memory controller provides control register bits for deassertion of each SDCKE pin.
SDCKE[1]	OC	SDRAM device clock enable. Connect SDCKE[1] to the clock enable pins of SDRAM. It is de-asserted (held low) during sleep. SDCKE[1] is always deasserted upon reset. The memory controller provides control register bits for deassertion of each SDCKE pin.
SDCLK[2:0]	OCZ	Use these clocks to clock synchronous memory devices: SDCLK0 - connected to either SMROM or synchronous flash devices SDCLK1 - connected to SDRAM banks 0/1 SDCLK2 - connected to SDRAM banks 2/3
nCS[5]/ GPIO[33]	ICOCZ	Static chip selects – These signals are chip selects to static memory devices such as ROM and flash. They are individually programmable in the memory configuration registers. nCS[5:0] may be used with variable data latency variable latency I/O devices. See Note [1]
nCS[4]/ GPIO[80]	ICOCZ	
nCS[3]/ GPIO[79]	ICOCZ	
nCS[2]/ GPIO[78]	ICOCZ	
nCS[1]/ GPIO[15]	ICOCZ	
nCS[0]	ICOCZ	Static chip select 0 – This is the chip select for the boot memory. nCS[0] is a dedicated pin (it is connected to the internal flash).
RD/nWR/GPIO[88]	ICOCZ	Read/Write for static interface – Intended for use as a steering signal for buffering logic
RDY/ GPIO[18]	ICOCZ	Variable Latency I/O Ready pin (input) See Note [1]
MBGNT/GP[13]	ICOCZ	Memory Controller grant – Output signal that notifies an external device that it has been granted the system bus.
MBREQ/GP[14]	ICOCZ	Memory Controller alternate bus master request – Input signal that is used by an external device to request the system bus from the Memory Controller.

Table 1-2. Signal Pin Descriptions (Sheet 3 of 8)

Name	Type	Description
PCMCIA/CF Control Pins		
nPOE/ GPIO[48]	ICOCZ	PCMCIA output enable – Output PCMCIA signal that performs reads from memory and attribute space. See Note [1]
nPWE/ GPIO[49]	ICOCZ	PCMCIA write enable – Output signal that performs writes to memory and attribute space. Also used as the write enable for VLIO. See Note [1]
nPIOW/ GPIO[51]	ICOCZ	PCMCIA I/O write – Output signal that performs write transactions to the PCMCIA I/O space. See Note [1]
nPIOR/ GPIO[50]	ICOCZ	PCMCIA I/O read – Output signal that performs read transactions from the PCMCIA I/O space. See Note [1]
nPCE[2:1]/ GPIO[53, 52]	ICOCZ	PCMCIA card enable – Output signals that selects a PCMCIA card. Bit one enables the high byte lane and bit zero enables the low byte lane. See Note [1]
nIOIS16/ GPIO[57]	ICOCZ	I/O Select 16 – Input signal from the PCMCIA card that indicates the current address is a valid 16-bit wide I/O address. See Note [1]
nPWAIT/ GPIO[56]	ICOCZ	PCMCIA wait – Input signal that is driven low by the PCMCIA card to extend the length of the transfers to/from the processor. See Note [1]
nPSKTSEL/ GPIO[54]	ICOCZ	PCMCIA socket select – Output signal used by external steering logic to route control, address, and data signals to one of the two PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. This signal has the same timing as address. See Note [1]
nPREG/ GPIO[55]	ICOCZ	PCMCIA register select – Output signal that indicates the target address is attribute space, on a memory transaction. This signal has the same timing as address. See Note [1]
LCD Controller Pins		
L_DD(15:0)/ GPIO[73:58]	ICOCZ	LCD Controller display data See Note [1]
L_FCLK/ GPIO[74]	ICOCZ	LCD Frame clock See Note [1]
L_LCLK/ GPIO[75]	ICOCZ	LCD Line clock See Note [1]
L_PCLK/ GPIO[76]	ICOCZ	LCD Pixel clock See Note [1]
L_BIAS/ GPIO[77]	ICOCZ	AC Bias Drive See Note [1]

Table 1-2. Signal Pin Descriptions (Sheet 4 of 8)

Name	Type	Description
Full Function UART Pins		
FFRXD/ GPIO[34]	ICOCZ	Full Function UART Receive pin See Note [1]
FFTXD/ GPIO[39]	ICOCZ	Full Function UART Transmit pin See Note [1]
FFCTS/ GPIO[35]	ICOCZ	Full Function UART Clear-to-Send pin See Note [1]
FFDCD/ GPIO[36]	ICOCZ	Full Function UART Data-Carrier-Detect pin See Note [1]
FFDSR/ GPIO[37]	ICOCZ	Full Function UART Data-Set-Ready pin: See Note [1]
FFRI/ GPIO[38]	ICOCZ	Full Function UART Ring Indicator pin See Note [1]
FFDTR/ GPIO[40]	ICOCZ	Full Function UART Data-Terminal-Ready pin See Note [1]
FFRTS/ GPIO[41]	ICOCZ	Full Function UART Ready-to-Send pin See Note [1]
Bluetooth UART Pins		
BTRXD/ GPIO[42]	ICOCZ	Bluetooth UART Receive pin See Note [1]
BTTXD/ GPIO[43]	ICOCZ	Bluetooth UART Transmit pin See Note [1]
BTCTS/ GPIO[44]	ICOCZ	Bluetooth UART Clear-to-Send pin See Note [1]
BTRTS/ GPIO[45]	ICOCZ	Bluetooth UART Data-Terminal-Ready pin See Note [1]
MMC Controller Pins		
MMCMD	ICOCZ	Multimedia Card Command pin (I/O)
MMDAT	ICOCZ	Multimedia Card Data Pin (I/O)
MMCLK/GP[6]	ICOCZ	MMC clock. (output) Clock signal for the MMC Controller.
MMCS0/GP[8]	ICOCZ	MMC chip select 0. (output) Chip select 0 for the MMC Controller.
MMCS1/GP[9]	ICOCZ	MMC chip select 1. (output) Chip select 1 for the MMC Controller.
SSP Pins		
SSPSCLK/ GPIO[23]	ICOCZ	Synchronous serial port clock (output) See Note [1]
SSPSFRM/ GPIO[24]	ICOCZ	Synchronous serial port frame signal (output) See Note [1]
SSPTXD/ GPIO[25]	ICOCZ	Synchronous serial port transmit (output) See Note [1]
SSPRXD/ GPIO[26]	ICOCZ	Synchronous serial port receive (input) See Note [1]

Table 1-2. Signal Pin Descriptions (Sheet 5 of 8)

Name	Type	Description
SSPEXTCLK/ GPIO[27]	ICOCZ	Synchronous serial port external clock (input) See Note [1]
USB Client Pins		
USB_P	IAOA	USB Client port positive Pin of differential pair.
USB_N	IAOA	USB Client port negative Pin of differential pair.
Single Ended USB Pins		
USB_RCV/GPIO[9]	ICOCZ	USB client single-ended interface RCV. Input from external transceiver to USB Device Controller.
USB_VP/GPIO[32]	ICOCZ	USB client single-ended interface VP. Input from external transceiver to USB Device Controller.
USB_VM/GPIO[34]	ICOCZ	USB client single-ended interface VM. Input from external transceiver to USB Device Controller.
USB_VPO/ GPIO[39]	ICOCZ	USB client single-ended interface VPO. Output to external transceiver differential driver.
USB_VMO/ GPIO[56]	ICOCZ	USB client single-ended interface VMO. Output to external transceiver differential driver.
USB_nOE/ GPIO[57]	ICOCZ	USB client single-ended interface nOE. Output enable to external transceiver.
AC97 Controller Pins		
BITCLK/ GPIO[28]	ICOCZ	AC97 Audio Port bit clock. (input) AC97 clock is generated by Codec 0 and fed into the PXA26x processor family processor and Codec 1. AC97 Audio Port bit clock. (output) AC97 clock is generated by the PXA26x processor family processor. I ² S bit clock. (input) I ² S clock is generated externally and fed into PXA26x processor family processor. I ² S bit clock. (output) I ² S clock is generated by the PXA26x processor family processor.
SDATA_IN0/ GPIO[29]	ICOCZ	AC97 Audio Port data in. (input) Input line for Codec 0. I ² S data in. (input) Input line for the I ² S Controller.
SDATA_IN1/ GPIO[32]	ICOCZ	AC97 Audio Port data in. (input) Input line for Codec 1. I ² S system clock. (output) System clock from I ² S Controller.
SDATA_OUT/ GPIO[30]	ICOCZ	AC97 Audio Port data out. (output) Output from the PXA26x processor family processor to Codecs 0 and 1. I ² S data out. (output) Output line for the I ² S Controller.
SYNC/ GPIO[31]	ICOCZ	AC97 Audio Port sync signal. (output) Frame sync signal for the AC97 Controller. I ² S sync. (output) Frame sync signal for the I ² S Controller.
nACRESET/ GPIO[89]	ICOC	AC97 Audio Port reset signal. (output)
Standard UART and ICP Pins		
IRRXD/ GPIO[46]	ICOCZ	IrDA receive signal (input). See Note [1]
IRTXD/ GPIO[47]	ICOCZ	IrDA transmit signal (output) – Transmit pin for both the SIR and FIR functions. See Note [1]

Table 1-2. Signal Pin Descriptions (Sheet 6 of 8)

Name	Type	Description
I²C Controller Pins		
SCL	ICOCZ	I ² C clock – Bi-directional signal. When it is driving, it functions as an open collector device and requires a pull up resistor. As an input, it expects standard CMOS levels.
SDA	ICOCZ	I ² C Data signal – Bi-directional signal. When it is driving, it functions as an open collector device and requires a pull up resistor. As an input, it expects standard CMOS levels.
PWM Pins		
PWM[1:0]/ GPIO[17,16]	ICOCZ	Pulse width modulation channels 0 and 1 (outputs) See Note [1]
Dedicated GPIO Pins		
GPIO[1:0]	ICOCZ	General Purpose I/O – Preconfigured at a hard reset (nRESET) as wakeup sources for both rising and falling edge detects. These GPIOs do not have alternate functions and are intended to be used as the main external sleep wake up stimulus.
GPIO[14:2])	ICOCZ	General Purpose I/O
GPIO[22:21]	ICOCZ	General Purpose I/O – Additional general purpose I/O pins.
GPIO[85]	ICOCZ	General Purpose I/O
Crystal Pins		
PXTAL	IA	Input connection for 3.6864 MHz crystal
PEXTAL	OA	Output connection for 3.6864 MHz crystal
TXTAL	IA	Input connection for 32.768 kHz crystal
TEXTAL	OA	Output connection for 32.768 kHz crystal
48MHz/GP[7]	ICOCZ	48 MHz clock – Peripheral clock output derived from the PLL.
RTCCLK/GP[10]	ICOCZ	Real time clock – Hz output derived from the 32 kHz or 3.6864 MHz output.
3.6MHz/GP[11]	ICOCZ	3.6864 MHz clock – Output from 3.6864 MHz oscillator.
32kHz/GP[12]	ICOCZ	32 kHz clock – Output from the 32 kHz oscillator.
Miscellaneous Pins		
BOOT_SEL [2:0]	IC	Boot programming select pins. These pins are sampled to indicate the type of boot device present per the following table: BOOT_SEL[2:0] Description 001 Asynchronous 16-bit ROM
PWR_EN	OC	Power Enable. Active high output – PWR_EN enables the external power supply. Negating it signals the power supply that the system is going into sleep mode and that the VDD power supply should be removed.
nBATT_FAULT	IC	Battery Fault. Active low input – The assertion of nBATT_FAULT causes the processor to enter sleep mode. The processor will not recognize a wakeup event while this signal is asserted. Use nBATT_FAULT signal to flag a critical power failure, such as removing the main battery. Minimum assertion time for nBATT_FAULT is 1ms.
nVDD_FAULT	IC	VDD Fault. Active low input – nVDD_FAULT causes the processor to enter sleep mode. nVDD_FAULT is ignored after a wakeup event until the power supply timer completes (approximately 10 ms). Use the nVDD_FAULT signal to flag a low battery. Minimum assertion time for nVDD_FAULT is 1 ms.

Table 1-2. Signal Pin Descriptions (Sheet 7 of 8)

Name	Type	Description
nRESET	IC	Hard reset. Active low input – nRESET is a level sensitive input which starts the processor from a known address. A LOW level causes the current instruction to terminate abnormally, and all on-chip state to be reset. When nRESET is driven HIGH, the processor re-starts from address 0. nRESET must remain LOW until the power supply is stable and the internal 3.6864 MHz oscillator has come up to speed. While nRESET is LOW the processor performs idle cycles.
nRESET_OUT	OC	Reset Out. Active low output – This signal is asserted when nRESET is asserted and de-asserts after nRESET is negated but before the first instruction fetch. nRESET_OUT is also asserted for “soft” reset events (sleep, watchdog reset, GPIO reset)
JTAG Pins		
nTRST	IC	JTAG Test Interface Reset. Resets the JTAG/Debug port – If JTAG/Debug is used, drive nTRST from low to high either before or at the same time as nRESET. If JTAG is not used, nTRST must be either tied to nRESET or tied low. Intel recommends that a JTAG/Debug port be added to all systems for debug and download. See Chapter 9 for details.
TDI	IC	JTAG test interface data input – This pin has an internal pullup resistor.
TDO	OCZ	JTAG test interface data output – This pin does NOT have an internal pullup resistor.
TMS	IC	JTAG test interface mode select – This pin has an internal pullup resistor.
TCK	IC	JTAG test interface reference Clock – TCK is the reference clock for all transfers on the JTAG test interface. NOTE: This pin needs an external pulldown resistor.
TEST	IC	Test Mode – Ground this pin on the PCB. This pin is for manufacturing purposes only.
TESTCLK	IC	Test Clock – Use this pin for test purposes only. An end user should ground this pin.
Power and Ground Pins		
VCC	SUP	Positive supply for the internal logic. Connect this supply to the low voltage (.85 - 1.65v) supply on the PCB.
VSS	SUP	Ground supply for the internal logic. Connect these pins to the common ground plane on the PCB.
PLL_VCC	SUP	Positive supply for PLLs and oscillators must be shorted to VCC.
PLL_VSS	SUP	Ground supply for the PLL. It must be connected to common ground plane on the PCB.
VCCQ	SUP	Positive supply for all CMOS I/O except memory bus and PCMCIA pins. Connect these pins to the common 2.775 V or 3.3 V supply on the PCB.
VSSQ	SUP	Ground supply for all CMOS I/O except memory bus and PCMCIA pins. Connect these pins to the common ground plane on the PCB.
VCCN	SUP	Positive supply for memory bus and PCMCIA pins. Connect these pins to the common 3.3 V, 2.775 V, or 2.5 V supply on the PCB.
VSSN	SUP	Ground supply for memory bus and PCMCIA pins. Connect these pins to the common ground plane on the PCB.
Network SSP Pins		
NSSPSCLK/ GPIO[81]	ICOCZ	Network synchronous serial port clock (output) See Note [1]
NSSPSFRM/ GPIO[82]	ICOCZ	Network synchronous serial frame signal (output) See Note [1]
NSSPTXD/ GPIO[83]	ICOCZ	Network Synchronous serial port transmit (output) See Note [1]

Table 1-2. Signal Pin Descriptions (Sheet 8 of 8)

Name	Type	Description
NSSPRXD/ GPIO[84]	ICOCZ	Network Synchronous serial port receive (input) See Note [1]
HWUART Pins		
HWTXD/GPIO[48]	ICOCZ	Hardware UART transmit data See Note [1]
HWRXD/GPIO[49]	ICOCZ	Hardware UART receive data See Note [1]
HWCTS/GPIO[50]	ICOCZ	Hardware UART clear-to-send See Note [1]
HWRTS/GPIO[51]	ICOCZ	Hardware UART request-to-send See Note [1]
Audio SSP Pins		
ASSPSCLK/ GPIO[28]	ICOCZ	Audio synchronous serial port clock (output) See Note [1]
ASSPSFRM/ GPIO[31]	ICOCZ	Audio synchronous serial port frame signal (output) See Note [1]
ASSPTXD/ GPIO[30]	ICOCZ	Audio synchronous serial port transmit (output) See Note [1]
ASSPRXD/ GPIO[29]	ICOCZ	Audio synchronous serial port receive (input) See Note [1]
Flash Specific Pins		
nRST_F	IC	Reset for flash only
nWP	IC	Write protect
VPEN	IC	Erase/Program/Block Lock Enable
WAIT_F1/WAIT_F2	OCZ	Wait – Indicates invalid data in synchronous-read (burst) modes.
VCC_F	SUP	Flash Core Logic Supply
VSS_F	SUP	Flash Core Ground
VCCQ_F	SUP	Flash I/O Power Supply – Must be the same voltage as VCCN.
VSSQ_F	SUP	Flash I/O Ground

NOTE: GPIO Reset Operation: After any reset, these pins are configured as GPIO inputs by default. The input buffers for these pins are disabled to prevent current drain and must be enabled prior to use by clearing the Read Disable Hold (RDH) bit.

NOTE: To use a GPIO pin as an alternate function, follow this sequence:

1. Program the pin to the desired direction (input or output) using the GPIO Pin Direction Registers (GPDR).
2. Enable the input buffer by clearing the RDH bit, described above.
3. If needed, select the desired alternate function by programming the proper bits in the GPIO Alternate Function Register (GAFR).

Figure 1-2. Intel® PXA26x Processor Family

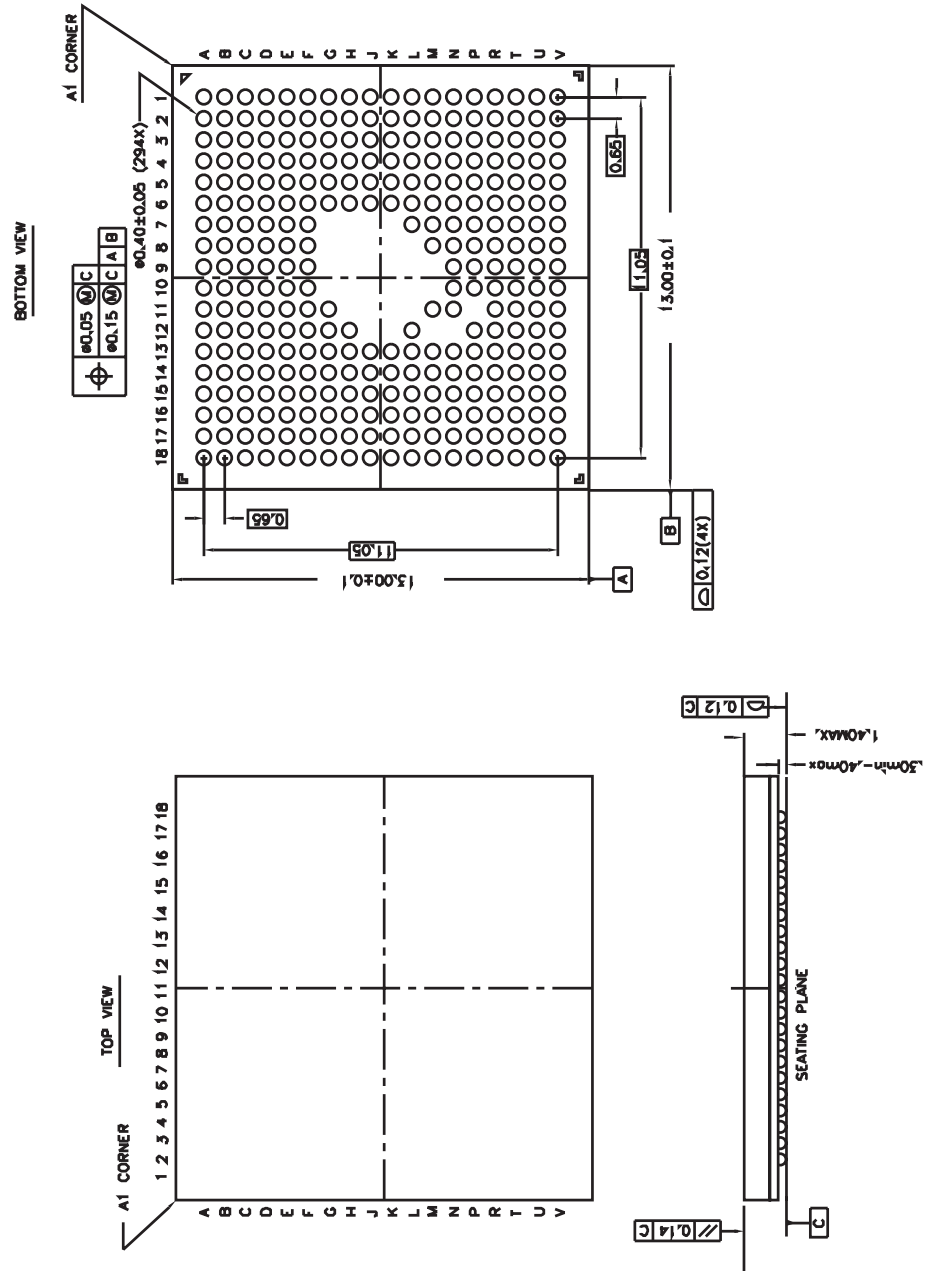


Table 1-3. Intel® PXA26x Processor Family Pin Out - Ballpad Number Order (Sheet 1 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	VSSN	G1	nSDCS[1]	P13	MD[14]
A2	VSSN	G2	nSDRAS	P14	MD[15]
A3	GPIO[69]	G3	VCCN	P15	GPIO[48]
A4	GPIO[13]	G4	nSDCS[0]	P16	VSSQ
A5	VCC	G5	nSDCAS	P17	VCC
A6	GPIO[63]	G6	VSSN	P18	GPIO[21]
A7	GPIO[11]	G11	VCC_F	R1	VCCN
A8	GPIO[76]	G12	BOOT_SEL[2]	R2	VCC
A9	VSSQ	G13	BOOT_SEL[1]	R3	MA[20]
A10	GPIO[24]	G14	BOOT_SEL[0]	R4	MA[23]
A11	GPIO[30]	G15	TEST	R5	MA[25]
A12	GPIO[38]	G16	TESTCLK	R6	VCCN
A13	SDA	G17	nTRST	R7	VSSQ
A14	VCCQ	G18	GPIO[6]	R8	MD[6]
A15	USB_P	H1	VSSQ	R9	nCS0
A16	GPIO[42]	H2	VCCN	R10	VSSN
A17	VSSQ	H3	MA[0]	R11	MD[11]
A18	VSSQ	H4	VSSN	R12	VCCQ_F
B1	VSSN	H5	nSDCS[2]/GPIO[86]	R13	VSSQ_F
B2	VSSN	H6	MA[1]	R14	VCC
B3	GPIO[71]	H12	TMS	R15	VCCN
B4	GPIO[66]	H13	TCK	R16	GPIO[50]
B5	VSSQ	H14	GPIO[5]	R17	GPIO[53]
B6	GPIO[64]	H15	PLL_VCC	R18	GPIO[19]
B7	GPIO[59]	H16	PLL_VSS	T1	MA[19]
B8	GPIO[77]	H17	TDO	T2	VCCN
B9	VCCQ	H18	TDI	T3	VSSQ
B10	GPIO[25]	J1	VSSQ	T4	MD[23]
B11	GPIO[29]	J2	VCC	T5	MA[24]
B12	GPIO[16]	J3	VSSN	T6	MD[24]
B13	GPIO[37]	J4	MD[16]	T7	VSSN
B14	VSSQ	J5	VCCN	T8	MD[5]
B15	USB_N	J6	MA[2]	T9	MD[26]
B16	GPIO[47]	J13	GPIO[4]	T10	DQM[0]
B17	VSSQ	J14	nRESET	T11	VCCN
B18	VSSQ	J15	nRESET_OUT	T12	MD[28]

Table 1-3. Intel® PXA26x Processor Family Pin Out - Ballpad Number Order (Sheet 2 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C1	DQM[2]	J16	nBATT_FAULT	T13	VCCN
C2	GPIO[73]	J17	VCC	T14	VSSN
C3	GPIO[70]	J18	VSSQ	T15	MD[13]
C4	GPIO[67]	K1	MD[17]	T16	GPIO[20]
C5	VSSQ	K2	MA[3]	T17	GPIO[51]
C6	GPIO[65]	K3	MA[4]	T18	GPIO[52]
C7	GPIO[61]	K4	MA[5]	U1	VSSN
C8	GPIO[75]	K5	MA[6]	U2	VSSN
C9	GPIO[74]	K6	MD[18]	U3	VSS
C10	GPIO[26]	K13	GPIO[3]	U4	VCCN
C11	GPIO[31]	K14	PEXTAL	U5	MA[22]
C12	GPIO[17]	K15	TEXTAL	U6	MD[3]
C13	GPIO[36]	K16	TXTAL	U7	MD[2]
C14	GPIO[35]	K17	PWR_EN	U8	MD[4]
C15	GPIO[34]	K18	nVDD_FAULT	U9	VSSN
C16	GPIO[45]	L1	VCCN	U10	GPIO[15]
C17	GPIO[46]	L2	MA[7]	U11	GPIO[79]
C18	VCC	L3	VSSN	U12	MD[10]
D1	SDCKE[0]	L4	MA[9]	U13	VSSQ
D2	GPIO[18]	L5	MA[8]	U14	MD[31]
D3	GPIO[72]	L6	MA[10]	U15	MD[12]
D4	GPIO[68]	L7	MA[14]	U16	GPIO[33]
D5	VCCQ	L12	nOE	U17	VSSN
D6	GPIO[12]	L13	nWE	U18	VSSN
D7	GPIO[60]	L14	GPIO[55]	V1	VSSN
D8	GPIO[41]	L15	VCCQ	V2	VSSN
D9	GPIO[23]	L16	VSSQ	V3	VCCN
D10	GPIO[28]	L17	GPIO[2]	V4	MA[21]
D11	nACRESET/GPIO[89]	L18	PXTAL	V5	VSSN
D12	VCC	M1	MA[11]	V6	MD[1]
D13	GPIO[39]	M2	MD[19]	V7	VCCN
D14	GPIO[43]	M3	VCCN	V8	VCC
D15	GPIO[44]	M4	VSSN	V9	MD[7]
D16	GPIO[9]	M5	MA[15]	V10	DQM[3]
D17	VCCQ	M6	VSSQ_F	V11	GPIO[78]
D18	VSS	M7	VCCQ_F	V12	MD[9]
E1	nSDCLK[2]	M8	VCC_F	V13	MD[29]
E2	RDnWR/GPIO[88]	M11	VSS_F	V14	MD[30]

Table 1-3. Intel® PXA26x Processor Family Pin Out - Ballpad Number Order (Sheet 3 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
E3	VCCN	M13	VCCQ_F	V15	VSSN
E4	DQM[1]	M14	WAIT_F1	V16	GPIO[80]
E5	GPIO[14]	M15	GPIO[56]	V17	VSSN
E6	GPIO[62]	M16	GPIO[22]	V18	VSSN
E7	GPIO[58]	M17	GPIO[1]		
E8	GPIO[10]	M18	GPIO[0]		
E9	GPIO[27]	N1	MD[20]		
E10	GPIO[40]	N2	MA[13]		
E11	SCL	N3	MA[12]		
E12	VSSQ	N4	MD[22]		
E13	MMDAT	N5	MA[17]		
E14	GPIO[32]	N6	VSSQ_F		
E15	MMCCMD	N7	VCCQ_F		
E16	GPIO[84]	N8	VCC_F		
E17	GPIO[81]	N9	MD[27]		
E18	GPIO[85]	N10	NC		
F1	nSDCS[3]/GPIO[87]	N11	VCCQ_F		
F2	VCC	N13	VSSQ_F		
F3	SDCLK[1]	N14	WAIT_F2		
F4	SDCKE[1]	N15	GPIO[49]		
F5	SDCLK[0]	N16	VCCN		
F6	VSS_F	N17	GPIO[54]		
F7	VSS_F	N18	GPIO[57]		
F8	nRST_F	P1	VSSQ		
F9	nWP_F	P2	MD[21]		
F10	VPEN_F	P3	MA[16]		
F11	VCC_F	P4	VCCQ_F		
F12	VSSQ_F	P5	MA[18]		
F13	GPIO[8]	P6	MD[0]		
F14	GPIO[82]	P7	MD[25]		
F15	GPIO[83]	P8	VCCN		
F16	GPIO[7]	P9	MD[8]		
F17	VCCQ	P10	VSS_F		
F18	VSSQ	P12	VCCQ_F		

This section is the design guidelines for the system memory interface.

2.1 Overview

The external memory bus interface for the processor supports:

- 100 MHz SDRAM
- Synchronous and asynchronous Burst mode and Page mode flash
- Synchronous Mask ROM (SMROM)
- Page Mode ROM
- SRAM
- SRAM-like Variable Latency I/O (VLIO)
- PCMCIA expansion memory
- Compact Flash

Internally, the Intel® PXA26x Processor Family contains one of the following non-SDRAM-timing synchronous flash memory configurations.

- PXA261 processor - 128 Mb x16
- PXA262 processor - 256 Mb x16

Use the memory interface configuration registers to program the memory types. Refer to Figure 1-1, “Processor Block Diagram” on page 1-2 for the block diagram of the Memory Controller configuration. Refer to Table 2-1 for the processor memory map. Refer to Table 2-3 for alternate mode address mapping.

Figure 2-1. General Memory Interface Configuration

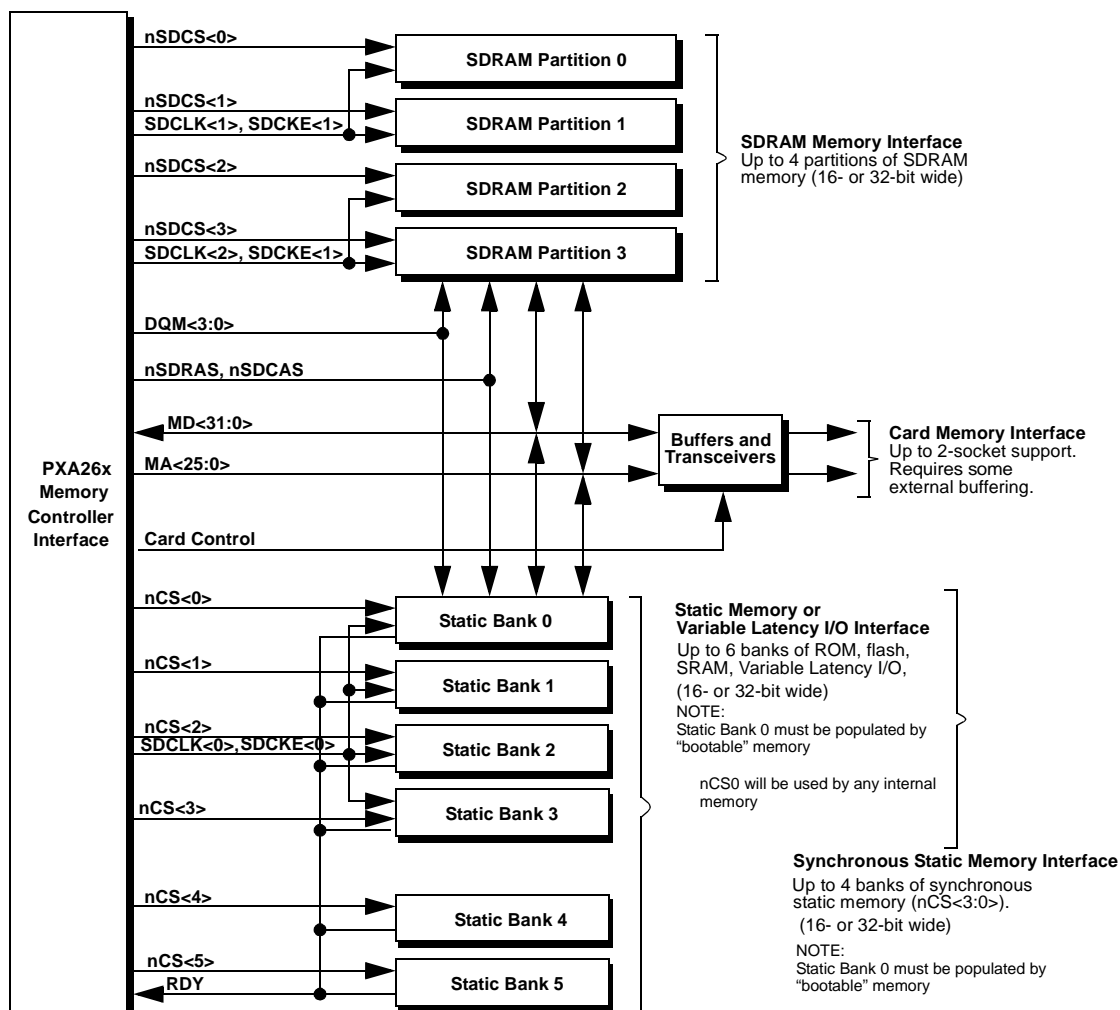


Table 2-1. Memory Address Map

0x6000_0000	reserved address space
0x5C00_0000	reserved address space
0x5800_0000	reserved address space
0x5400_0000	reserved address space
0x5000_0000	reserved address space
0x4C00_0000	reserved address space
0x4800_0000	Memory mapped registers (memory Ctl)
0x4400_0000	Memory mapped registers (LCD)
0x4000_0000	Memory mapped registers (peripherals)
0x3000_0000	PCMCIA/CF – Slot 1
0x2000_0000	PCMCIA/CF – Slot 0
0x1C00_0000	reserved address space
0x1800_0000	reserved address space
0x1400_0000	Static Chip Select 5
0x1000_0000	Static Chip Select 4
0x0C00_0000	Static Chip Select 3
0x0800_0000	Static Chip Select 2
0x0400_0000	Static Chip Select 1
0x0000_0000	Static Chip Select 0

2.1.1 Internal Flash Connections

Figure 2-2 and Figure 2-3 show the internal connections for each flash memory configuration of the PXA26x processor family.

Figure 2-2. PXA261 Processor Internal Configuration

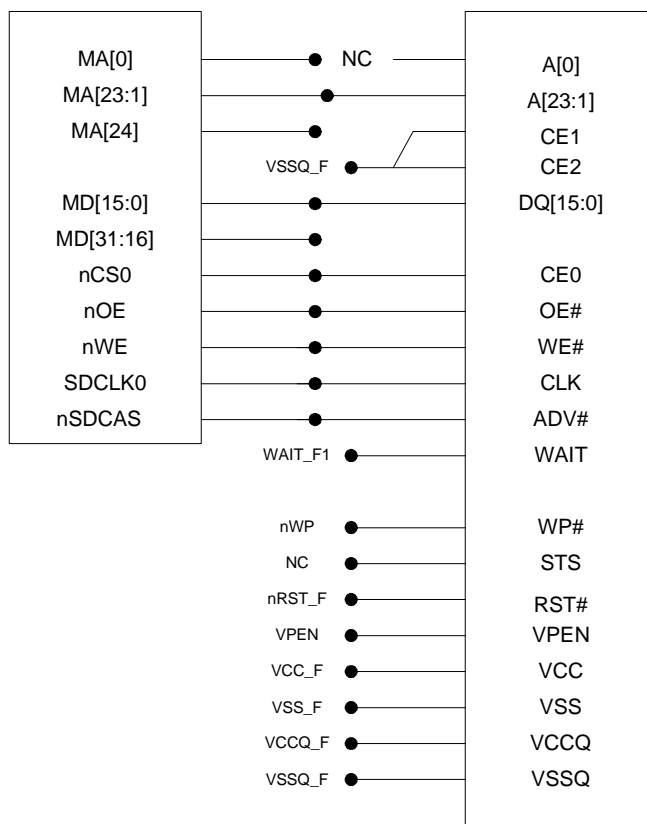
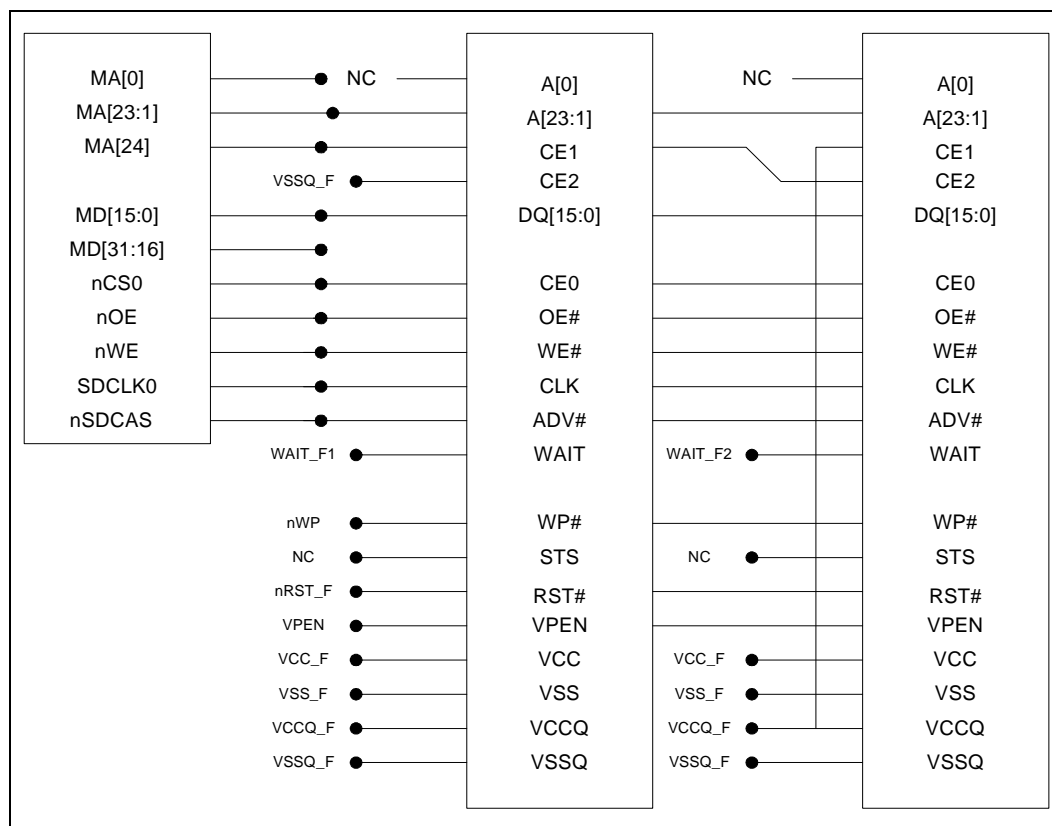


Figure 2-3. PXA262 Processor Internal Configuration



2.2 SDRAM Interface

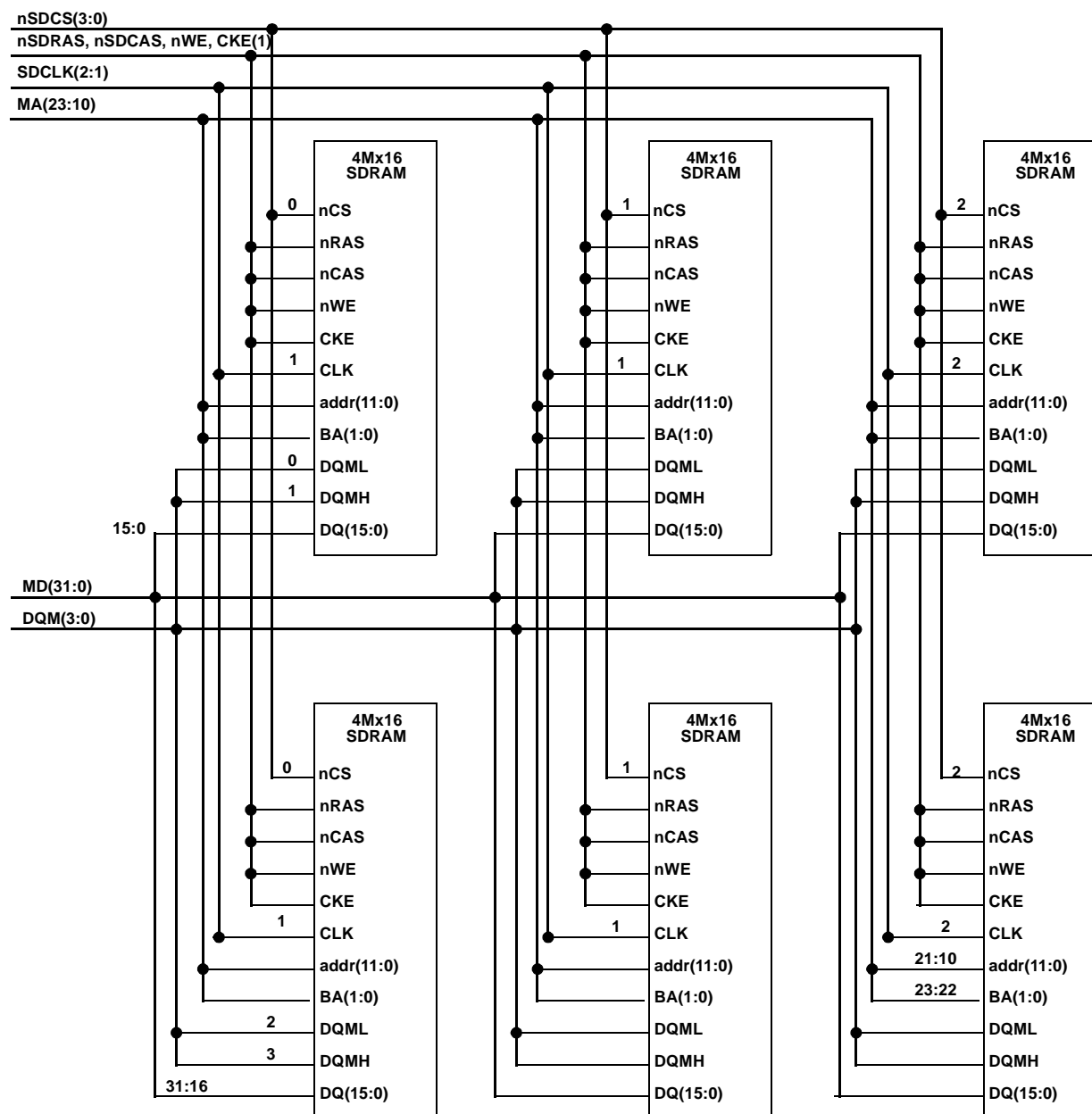
The processor supports an SDRAM interface at a maximum frequency of 100 MHz. The SDRAM interface supports four 16-bit or 32-bit wide SDRAM partitions. Each partition is allocated 64 MBytes of the internal memory map. However, the actual size of each partition is dependent on the particular SDRAM configuration used. The four partitions are divided into two partition pairs: the 0/1 pair and the 2/3 pair. Both partitions within a pair (for example, partition 0 and partition 1) must be identical in size and configuration; however, the two pairs can be different. For example, the 0/1 pair can be 100 MHz SDRAM on a 32-bit data bus, while the 2/3 pair can be 50 MHz SDRAM on a 16-bit data bus.

Note: For proper SDRAM operation above 50 MHz, 22 ohm series resistors must be placed on the memory address, data and control lines.

2.3 SDRAM memory wiring diagram

Figure 2-4 is a wiring diagram example that shows a system using 1 Mword x 16-bit x 4-bank SDRAM devices for a total of 48 Mbytes. Refer to Section 2.5 to determine the individual SDRAM component address.

Figure 2-4. SDRAM Memory System Example



2.4 SDRAM Support

Table 2-2 shows the SDRAM memory types and densities that are supported by the processor.

Table 2-2. SDRAM Memory Types Supported by the Processor

Partition Size (Mbyte/Partition)		SDRAM Configuration (Words x Bits)	Chip Size	Number Chips/ Partition		Bank Bits x Row bits x Column Bits	Maximum Memory (4 Partitions)		Total Number of Chips	
16-bit Bus	32-bit Bus			16-bit Bus	32-bit bus		16-bit Bus	32-bit Bus	16-bit Bus	32-bit Bus
2 Mbyte	4 Mbyte	1M x 16	16 Mbit	1	2	1 x 11 x 8	8 Mbyte	16 Mbyte	4	8
4 Mbyte	8 Mbyte	2 M x 8	16 Mbit	2	4	1 x 11 x 9	16 Mbyte	32 Mbyte	8	16
8 Mbyte	16 Mbyte	4 M x 4	16 Mbit	4	8	1 x 11 x 10	32 Mbyte	64 Mbyte	16	32
N/A	8 Mbyte	2 M x 32	64 Mbit	N/A	1	2 x 11 x 8	N/A	32 Mbyte	N/A	4
8 Mbyte	16 Mbyte	4 M x 16	64 Mbit	1	2	1 x 13 x 8 2 x 12 x 8	32 Mbyte	64 Mbyte	4	8
16 Mbyte	32 Mbyte	8 M x 8	64 Mbit	2	4	1 x 13 x 9 2 x 12 x 9	64 Mbyte	128 Mbyte	8	16
32 Mbyte	64 Mbyte	16 M x 4	64 Mbit	4	8	1 x 13 x 10 2 x 12 x 10	128 Mbyte	256 Mbyte	16	32
16 Mbyte	32 Mbyte	8 M x 16	128 Mbit	1	2	2 x 12 x 9	64 Mbyte	128 Mbyte	4	8
32 Mbyte	64 Mbyte	16 M x 8	128 Mbit	2	4	2 x 12 x 10	128 Mbyte	256 Mbyte	8	16
64 Mbyte	N/A	32 M x 4	128 Mbit	4	8	2 x 12 x 11	256 Mbyte	N/A	16	32
32 Mbyte	64 Mbyte	16 M x 16	256 Mbit	1	2	2 x 13 x 9	128 Mbyte	256 Mbyte	4	8
64 Mbyte	N/A	32 M x 8	256 Mbit	2	4	2 x 13 x 10	256 Mbyte	N/A	8	16

2.5 SDRAM Address Mapping

SDRAM address mapping is shown in Table 2-3 and Table 2-4.

Table 2-3. Normal Mode Memory Address Mapping

SDRAM		# Bits Bank x Row x Col	The processor pin mapping to SDRAM devices (The address lines at the top of the columns are the processor address lines)														
Device	Technology		A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1Mx16	16Mbit	1x11x8				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Mx8	16Mbit	1x11x9				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Mx4	16Mbit	1x11x10				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x8			BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x9			BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x10			BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x11			BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x8		BS0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x9		BS0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x10		BS0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x11		BS0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Mx32	64Mbit	2x11x8			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		2x11x9			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		2x11x10			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Mx16/ 4Mx32	64Mbit/ 128Mbit	2x12x8		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8Mx8/ 8Mx16	64Mbit/ 128Mbit	2x12x9		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16Mx4/ 16Mx8	64Mbit/ 128Mbit	2x12x10		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
32Mx4	128Mbit	2x12x11		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8Mx32	256Mbit	2x13x8	BS1	BS0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16Mx16	256Mbit	2x13x9	BS1	BS1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 2-4. Processor Compatibility Mode Address Line Mapping

SDRAM		# Bits Bank x Row x Col	The processor pin mapping to SDRAM devices (The address lines at the top of the columns are the processor address lines)														
Device	Technology		A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1Mx16	16Mbit	1x11x8				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Mx8	16Mbit	1x11x9				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Mx4	16Mbit	1x11x10				BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x8			A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x9			A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x10			A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x12x11			A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x8		A12	A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x9		A12	A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x10		A12	A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		1x13x11		A12	A11	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Mx32	64Mbit	2x11x8			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		2x11x9			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		2x11x10			BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Mx16/ 4Mx32	64Mbit/ 128Mbit	2x12x8		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8Mx8/ 8Mx16	64Mbit/ 128Mbit	2x12x9		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16Mx4/ 16Mx8	64Mbit/ 128Mbit	2x12x10		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
32Mx4	128Mbit	2x12x11		BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8Mx32	256Mbit	2x13x8	A12	BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16Mx16	256Mbit	2x13x9	A12	BS1	BS0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.6 Static Memory

2.6.1 Overview

The processor external memory bus interface supports these static memory types:

- Flash memory — Both asynchronous and synchronous accesses

- Synchronous mask ROM (SMROM)
- Page mode ROM
- SRAM
- SRAM-like Variable Latency I/O (VLIO)
- PCMCIA expansion memory
- Compact Flash

Memory types are programmable through the memory interface configuration registers.

Six chip selects control the static memory interface, $nCS<5:0>$. All are configurable for nonburst ROM or flash memory, burst ROM or flash, SRAM, or SRAM-like variable latency I/O devices. The variable latency I/O interface differs from SRAM in that it allows the data ready input signal (RDY) to insert a variable number of memory-cycle-wait states. The data bus width for each chip select region may be programmed to be 16-bit or 32-bit. $nCS<3:0>$ are also configurable for Synchronous Static Memory. $nCS0$ is connected to any internal flash, but it is also brought out of the package. The external $nCS0$ signal can be used for an external flash programmer.

For SRAM and variable latency I/O implementations, $DQM<3:0>$ signals are used for the write byte enables, where $DQM<3>$ corresponds to the MSB. The processor supplies 26-bits of byte address for access of up to 64 Mbytes per chip select. However, when the address is sent out on the MA pins, MA reflects the actual address, not the byte address. The lower one or two internal address bits are truncated appropriately.

2.6.2 Boot Time Defaults

Booting configuration is device specific. Table 2-5 shows valid booting configurations based on processor type, while Table 2-6 shows boot selection definitions. See the Intel® PXA26x Processor Family *Developer's Manual* for more detailed descriptions of these boot time configurations.

Table 2-5. Valid Booting Configurations Based on Package Type

Valid Booting Configurations
001

Table 2-6. BOOT_SEL Definitions

BOOT_SEL			Boot From . . .
2	1	0	
0	0	1	Asynchronous 16-bit ROM

2.6.3 Flash Memory

The processor supports flash memory on all six static chip selects and synchronous operation on $nCS[3:0]$. The internal flash is connected to $nCS0$ already.

2.6.3.1 Additional Flash Memory

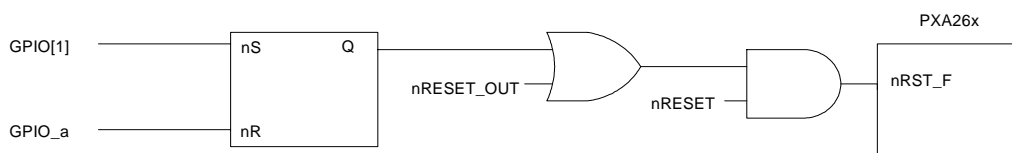
If additional synchronous flash memory is used in the system, the traces for SDCLK0, address, data and control should be limited to 3 inches. If the traces must exceed 3 inches, 47 ohm series termination resistors must be included.

The maximum number of external flash parts is limited to two.

2.6.3.2 Synchronous Intel StrataFlash® Memory Reset

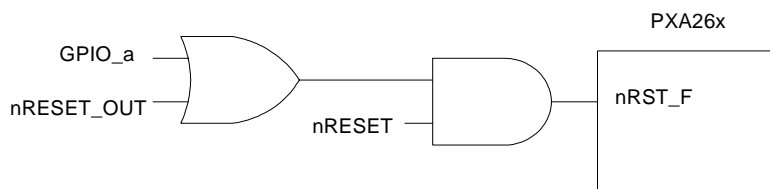
If nRESET_OUT is connected to nRST_F, Hardware reset, Watchdog reset and sleep mode work properly. GPIO reset does not work because the contents of the memory controller Synchronous Static Memory Configuration Register (SXCNFG) are not reset but the flash would be reset to asynchronous mode. If GPIO reset operation is required, a state machine is necessary between nRESET, nRESET_OUT, GPIO[1], and nRST_F to guarantee that nRST_F is asserted during hardware reset, watchdog reset, and sleep mode, and not asserted during GPIO reset. Figure 2-5 shows the required logic. GPIO_a is an unused GPIO that is driven low by software during the boot sequence and left high during normal operation. After this is completed, then enable GPIO Reset.

Figure 2-5. Flash Memory Reset Using State Machine



If watchdog reset is not necessary, a secondary GPIO can control nRESET_OUT using the equation $nRST_F = nRESET \& (nRESET_OUT \mid GPIO_a)$. This allows sleep mode entry to reset the flash memory while keeping it in synchronous mode during a GPIO reset. Figure 2-6 shows the required logic. GPIO_a is an unused GPIO that is kept high during normal operation and driven low before sleep mode entry.

Figure 2-6. Flash Memory Reset Logic if Watchdog Reset is Not Necessary



2.6.4 SRAM / ROM / Flash / Synchronous Fast Flash Memory Options

Table 2-7 contains the AC specification for SRAM / ROM / flash / synchronous fast flash.

Table 2-7. SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications

Symbol	Description	MEMCLK					Units Notes
		99.5	118.0	132.7	147.5	165.9	
SRAM / ROM / Flash / Synchronous Fast Flash (WRITES) (Asynchronous)							
tromAS	MA(25:0) setup to nOE, nSDCAS (as nADV) asserted	10	8.5	7.5	6.8	6	ns, 1
tromAH	MA(25:0) hold after nCS, nOE, nSDCAS (as nADV) de-asserted	10	8.5	7.5	6.8	6	ns, 1
tromASW	MA(25:0) setup to nWE asserted	30	25.5	22.5	20.4	18	ns, 3
tromAHW	MA(25:0) hold after nWE de-asserted	10	8.5	7.5	6.8	6	ns, 1
tromCES	nCS setup to nWE asserted	20	17	15	13.6	12	ns, 2
tromCEH	nCS hold after nWE de-asserted	10	8.5	7.5	6.8	6	ns, 1
tromDS	MD(31:0), DQM(3:0) write data setup to nWE asserted	10	8.5	7.5	6.8	6	ns, 1
tromDSWH	MD(31:0), DQM(3:0) write data setup to nWE de-asserted	20	17	15	13.6	12	ns, 2
tromDH	MD(31:0), DQM(3:0) write data hold after nWE de-asserted	10	8.5	7.5	6.8	6	ns, 1
tromNWE	nWE high time between beats of write data	20	17	15	13.6	12	ns, 2

NOTES:

1. This number represents 1 MEMCLK period
2. This number represents 2 MEMCLK periods

2.6.5 Variable Latency I/O Interface Overview

Both reads and writes for VLIO differ from SRAM in that the processor samples the data-ready input, RDY. The RDY signal is level sensitive and goes through a two-stage synchronizer on input. When the internal RDY signal is high, the I/O device is ready for data transfer. This means that for a transaction to complete at the minimum assertion time for either nOE or nPWE (RDF+1), the RDY signal must be high two clocks prior to the minimum assertion time for either nOE or nPWE (RDF-1). Data is latched on the rising edge of MEMCLK once the internal RDY signal is high and the minimum assertion time of RDF+1 has been reached. Once the data has been latched, the address may change on the next rising edge of MEMCLK or any cycles thereafter. The nOE or nPWE signal de-asserts one MEMCLK after data is latched. Before a subsequent data beat, nOE or nPWE remains deasserted for RDN+1 memory cycles. The chip select and byte selects, DQM[3:0], remain asserted for one memory cycle after the burst's final nOE or nPWE deassertion. Refer to Figure 2-7 for 32-Bit Variable Latency I/O read timing and Figure 2-8 for Variable Latency I/O interface AC specifications.

Figure 2-7. 32-Bit Variable Latency I/O Read Timing (Burst-of-Four, One Wait Cycle Per Beat)

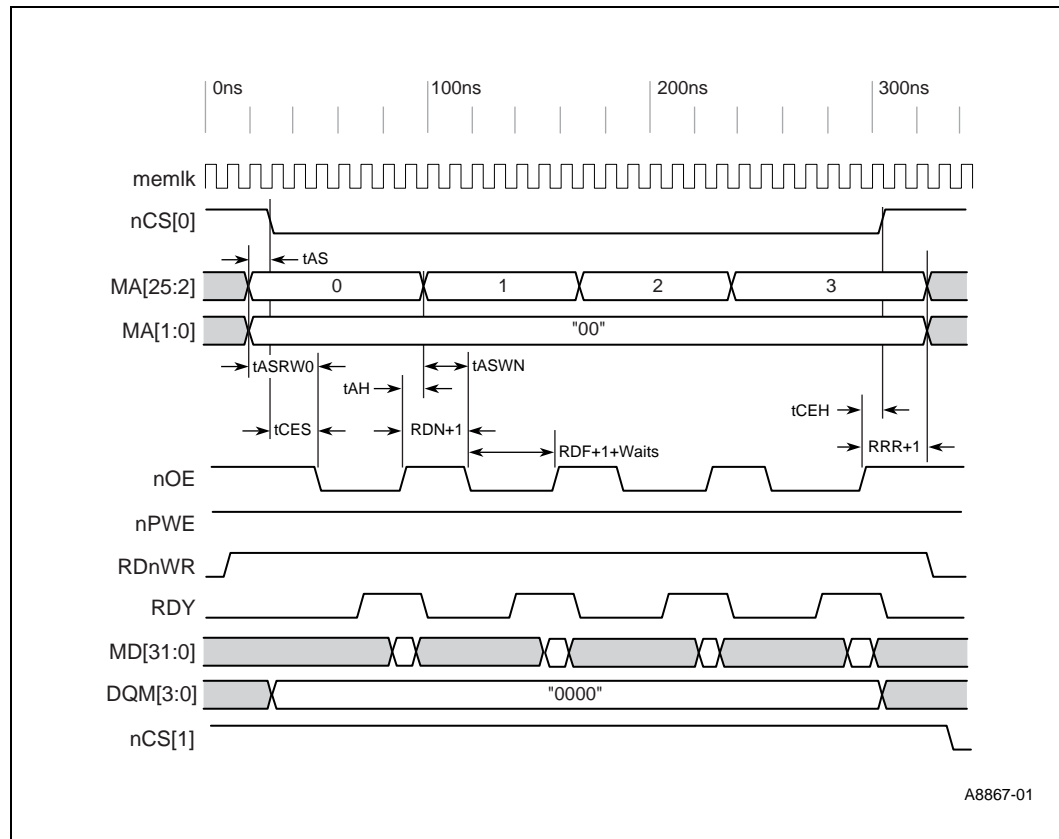


Table 2-8. Variable Latency I/O Interface AC Specifications (Sheet 1 of 2)

Symbol	Description	MEMCKLK					Units Notes
		99.5	118.0	132.7	147.5	165.9	
Variable Latency IO Interface (VLIO) (Asynchronous)							
tvlioAS	MA(25:0) setup to nCS asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioASRW	MA(25:0) setup to nOE or nPWE asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioAH	MA(25:0) hold after nOE or nPWE de-asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioCES	nCS setup to nOE or nPWE asserted	20	17	15	13.6	12	ns, 2
tvlioCEH	nCS hold after nOE or nPWE de-asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioDSW	MD(31:0), DQM(3:0) write data setup to nPWE asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioDSWH	MD(31:0), DQM(3:0) write data setup to nPWE de-asserted	20	17	15	13.6	12	ns, 2
tvlioDHW	MD(31:0), DQM(3:0) hold after nPWE de-asserted	10	8.5	7.5	6.8	6	ns, 1

Table 2-8. Variable Latency I/O Interface AC Specifications (Sheet 2 of 2)

Symbol	Description	MEMCLK					Units Notes
		99.5	118.0	132.7	147.5	165.9	
tvlioDHR	MD(31:0) read data hold after nOE de-asserted	0	0	0	0	0	ns
tvlioRDYH	RDY hold after nOE, nPWE de-asserted	0	0	0	0	0	ns
tvlioNPWE	nPWE, nOE high time between beats of write or read data	20	17	15	13.6	12	ns, 2

NOTES:

1. This number represents 1 MEMCLK period
2. This number represents 2 MEMCLK periods

2.6.6 External Logic for PCMCIA Implementation

The processor requires external glue logic to complete the PCMCIA socket interface. Figure 2-8 and Figure 2-9 show general solutions for one and two socket configurations. Use GPIO or memory-mapped external registers to control the PCMCIA interface's reset, power selection (V_{CC} and V_{pp}), and drive enables. These diagrams show the logical connections necessary to support hot insertion capability. For dual-voltage support, level shifting buffers are required for all the processor input signals. Hot insertion capability requires each socket be electrically isolated from the other and from the remainder of the memory system. If one or both of these features are not required, you may eliminate some of the logic shown in these diagrams. The processor allows either 1-socket or 2-socket solutions. In the 1-socket solution, only minimal glue logic is required (typically for the data transceivers, address buffers, and level shifting buffers.) To achieve this some of the signals are routed through dual-duty GPIO pins. The nOE of the transceivers is driven through the PSKTSEL pin, which is not needed in the one-socket solution. The DIR pin of the transceiver is driven through the RDnWR pin. A GPIO is used for the three-state signal of the address and nPWE lines. These signals are used for memories other than the card interface and must be three-stated.

Note: Level shifters are required if the Card does not drive within the PXA26x processor family VCCN specification.

In the 2-socket solution, all pins assume their normal duties and glue logic is necessary for proper operation of the system. The pull-ups shown are included for compliance with *PC Card Standard - Volume 2 - Electrical Specification*. Remove power from these pull-ups during sleep to avoid unnecessary power consumption. Refer to Table 2-9 for the PCMCIA or Compact Flash card interface AC specifications.

Figure 2-9. Expansion Card External Logic for a One-Socket Configuration

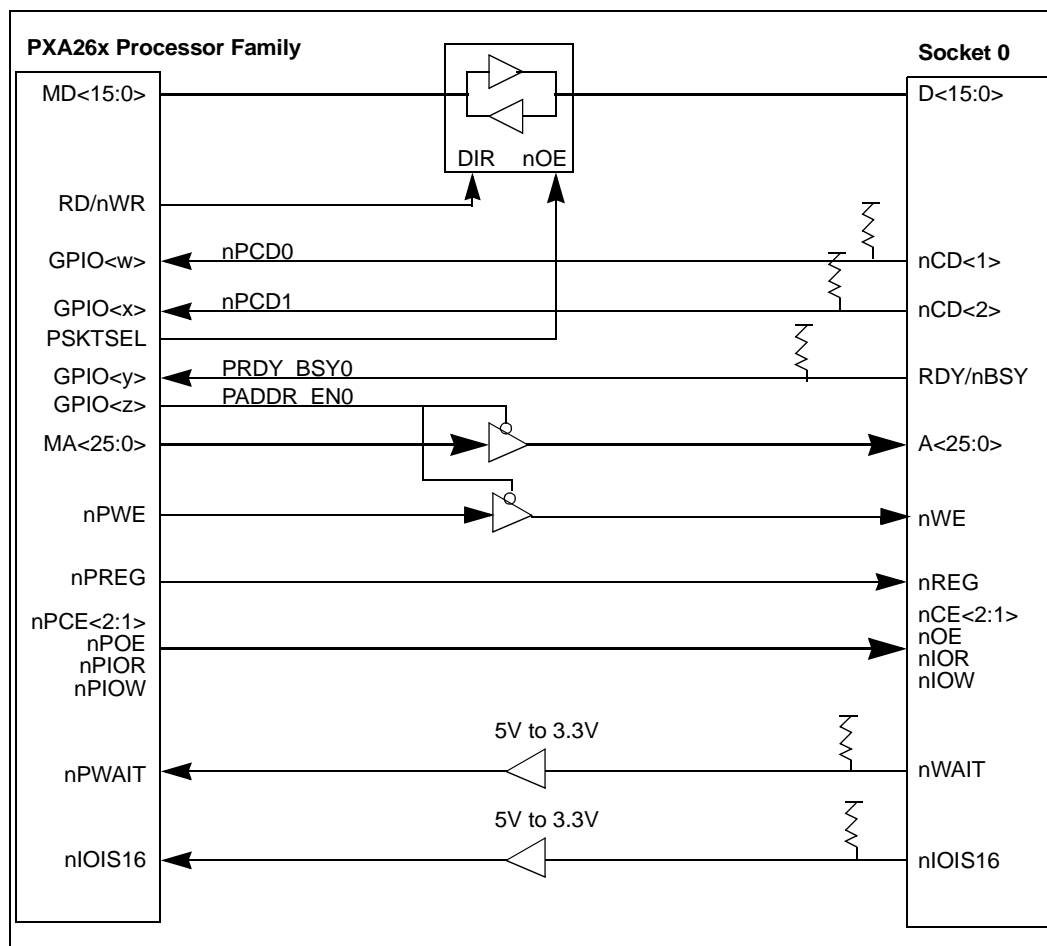


Table 2-9. Card Interface (PCMCIA or Compact Flash) AC Specifications (Sheet 1 of 2)

Symbol	Description	MEMCKLK					Units Notes
		99.5	118.0	132.7	147.5	165.9	
Card Interface (PCMCIA or Compact Flash) (Asynchronous)							
tcardAS	MA(25:0), nPREG, PSKTSEL, nPCE setup to nPWE, nPOE, nPIOW, or nPIOR asserted	20	17	15	13.6	12	ns, 1
tcardAH	MA(25:0), nPREG, PSKTSEL, nPCE hold after nPWE, nPOE, nPIOW, or nPIOR de-asserted	10	8.5	7.5	6.8	6	ns, 1
tcardDS	MD(31:0) setup to nPWE, nPOE, nPIOW, or NPIOR asserted	10	8.5	7.5	6.8	6	ns, 1

Table 2-9. Card Interface (PCMCIA or Compact Flash) AC Specifications (Sheet 2 of 2)

Symbol	Description	MEMCKLK					Units Notes
		99.5	118.0	132.7	147.5	165.9	
tcardDH	MD(31:0) hold after nPWE, nPOE, nPIOW, or NPIOR de-asserted	10	8.5	7.5	6.8	6	ns, 1
tcardCMD	nPWE, nPOE, nPIOW, or nPIOR command assertion	30	25.5	22.5	20.4	18	ns, 1

NOTE:

1. These numbers are minmums. They can be much larger based on the programmable Card Interface timing registers.

2.6.7 DMA / Companion Chip Interface

Connect a companion chip to the processor via:

- Alternate Bus Master Mode
- Variable Latency I/O
- Flow through DMA

These connections are illustrated in Figure 2-10 and Figure 2-11.

Figure 2-10. Alternate Bus Master Mode

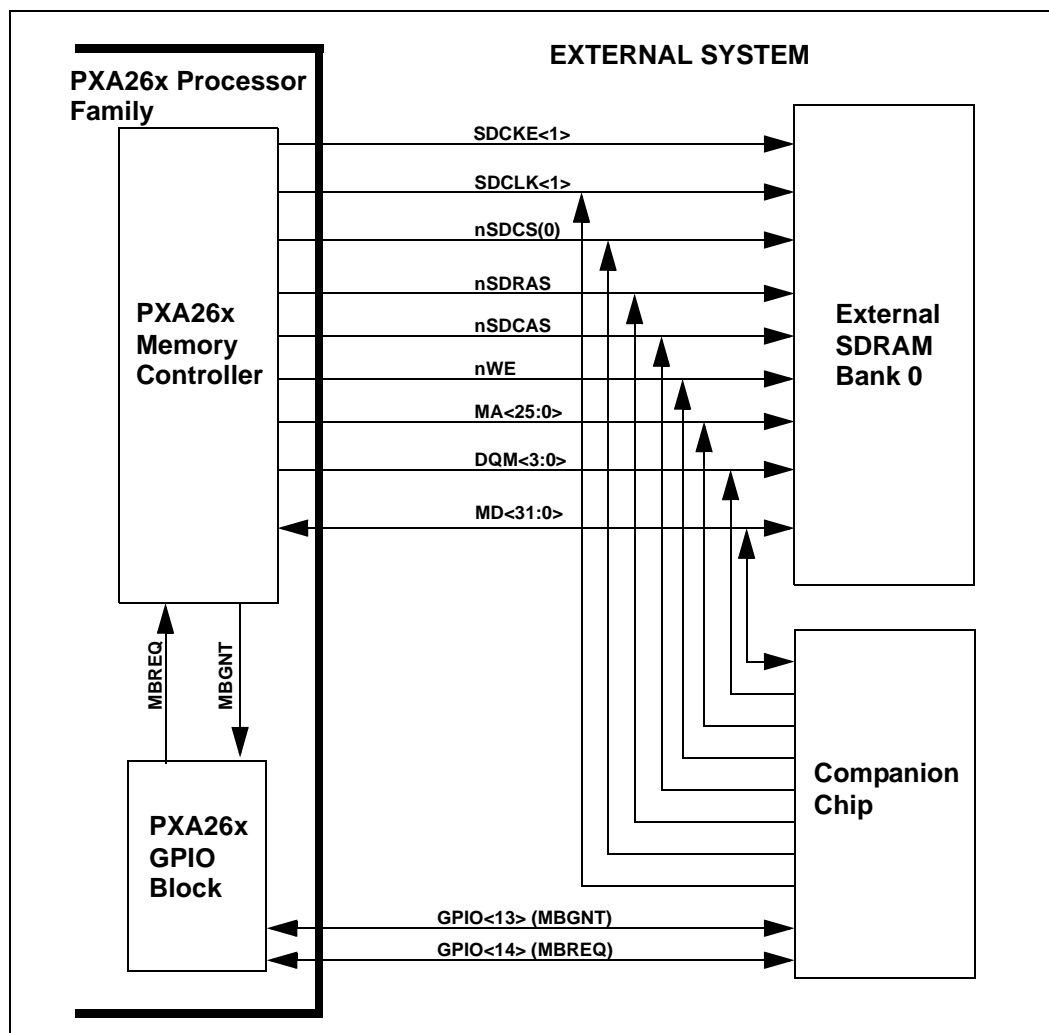
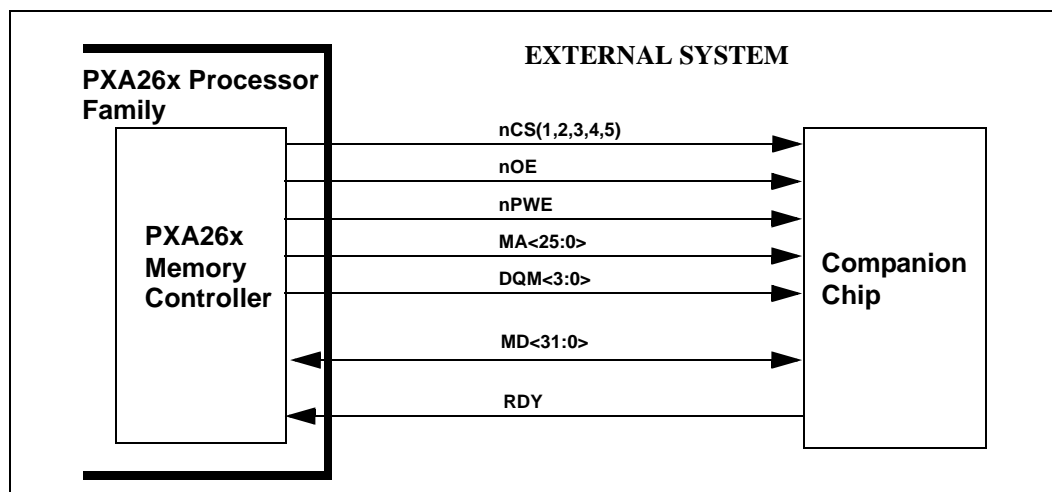


Figure 2-11. Variable Latency I/O



2.7 System Memory Layout Guidelines

2.7.1 System Memory Topologies (Min and Max Simulated Loading)

Figure 2-12, Figure 2-13, Figure 2-14, and Figure 2-15 are the topologies that were simulated to develop the trace length recommendations in Section 2.7.2. These topologies are for reference only.

Figure 2-12. CS, CKE, DQM, CLK, MA Minimum Loading Topology

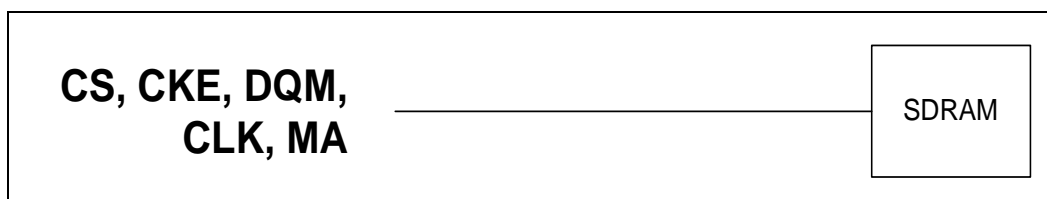


Figure 2-13. CS, CKE, DQM, CLK, MA Maximum Loading Topology

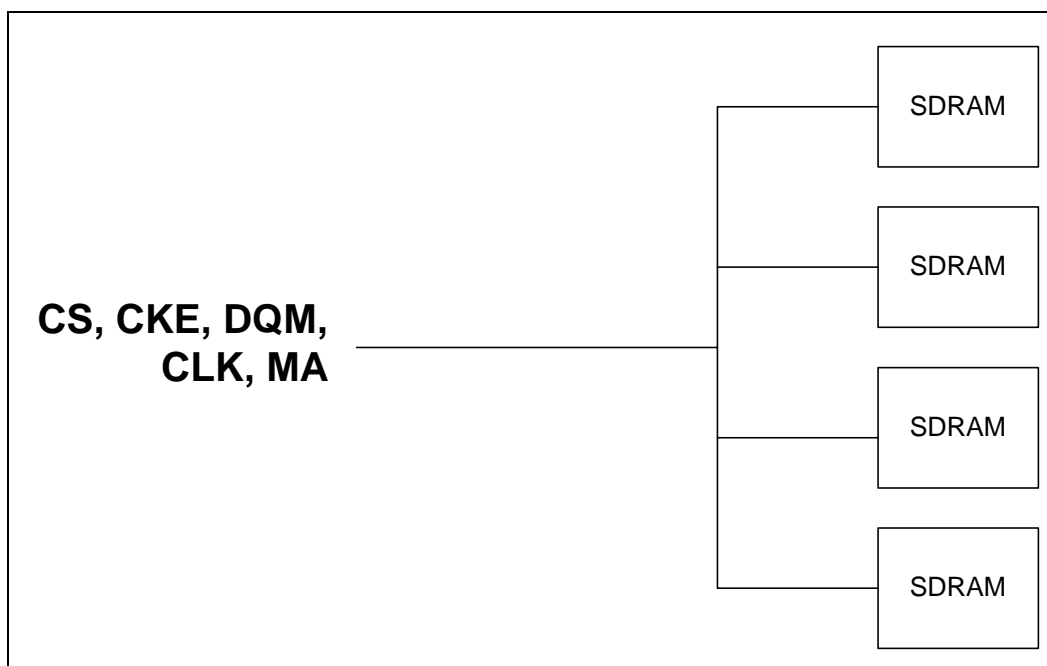


Figure 2-14. MD Minimum Loading Topology

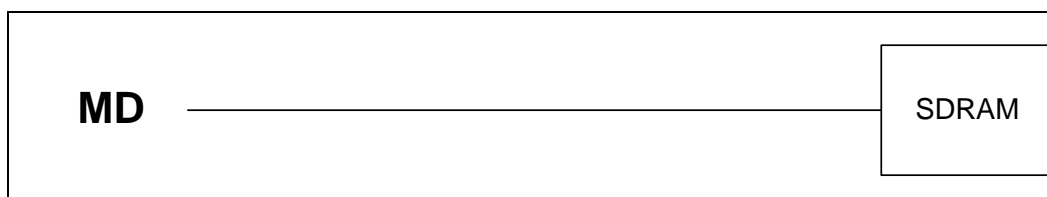
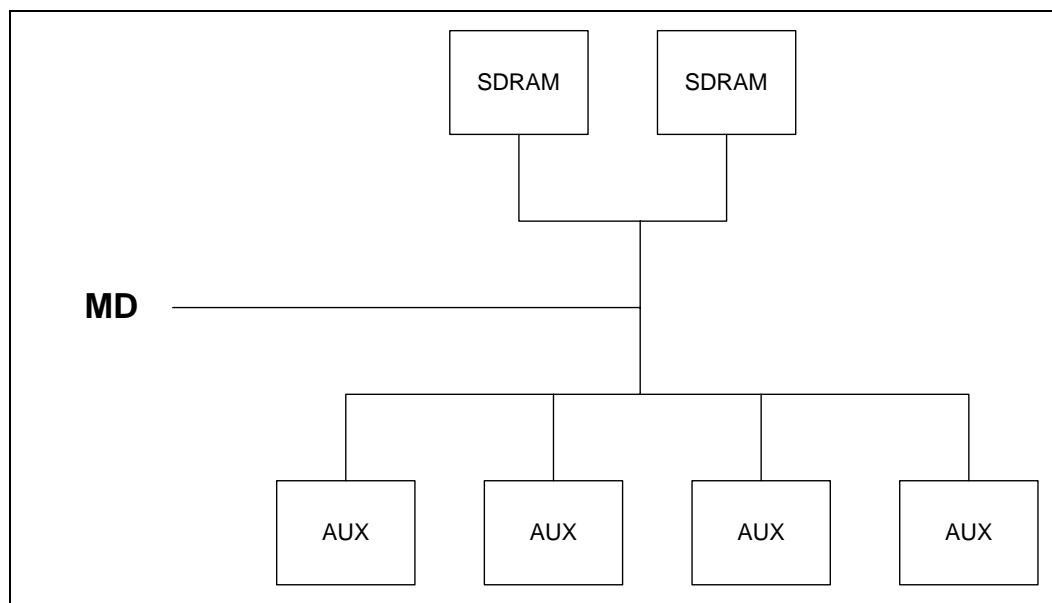


Figure 2-15. MD maximum Loading Topology



2.7.2 System Memory Recommended Trace Lengths

Table 2-10 details the minimum and maximum trace lengths that were simulated for the processor. These trace lengths are not the absolute trace lengths that will work given the loading conditions. The trace lengths in Table 2-10 are measured from the processor to the individual component pins. The board impedance for the simulations was 60 ohm +/- 10%.

Table 2-10. Minimum and Maximum Trace Lengths for the SDRAM Signals

Signal	Min Trace Length	Max Trace Length
CS, CKE, DQM	0.75 in	4.5 in
CLK	1.0 in	4.25 in
MA	1.0 in	4.5 in
MD	1.0 in	4.25 in

This chapter describes sample hardware connections from the Intel® PXA26x Processor Family to various types of LCD controllers. Active (TFT) as well as passive (DSTN) displays are discussed as well as single and dual panel displays. These should not be considered the only possible ways to connect an LCD panel to the PXA26x processor family, but should serve as a reference to assist with hardware design considerations. Other panels, for example panels without L_FCLK or L_LCLK, have been successfully connected to the processor.

3.1 LCD Display Overview

The PXA26x processor family supports both active and passive LCD displays. Active displays generally produce better looking images, but at a higher cost. Passive displays are generally less expensive, but their displays are inferior to active displays. However, recent advances in dithering technology are closing the quality gap between passive and active displays.

Note: Names used for “LCD Panel Pin” are representative names and may not match those on all LCD panels. Refer to the LCD panel reference documentation for the actual name.

3.2 Passive (DSTN) Displays

Several different types of passive displays are available in both color and monochrome. These maybe single or dual panel displays. Additionally, some monochrome displays use double-pixel data mode (twice the number of pixels as a normal monochrome display). With the exception of the number of data pins required, all of these choices affect the software configuration and support, not the system hardware design. In fact, most passive displays use a single interconnection scheme. For information on the software changes and performance considerations of the various display options, refer to the Intel® PXA26x Processor Family *Developer's Manual*.

Passive displays drive dithered data to the LCD panel - which means that for each pixel clock cycle a single data line drives an ON/OFF signal for one color of a single pixel.

Table 3-1 describes the number of L_DD pins required for the various types of passive displays, as well as which LCD data pins are used for which panel (upper or lower).

Table 3-1. LCD Controller Data Pin Utilization (Sheet 1 of 2)

Color/ Monochrome Panel	Single/ Dual Panel	Double-Pixel Mode	Screen Portion	Pins
Monochrome	Single	No	Whole	L_DD<3:0>
Monochrome	Single	Yes	Whole	L_DD<7:0> ¹
Monochrome	Dual	No	Top	L_DD<3:0>
			Bottom	L_DD<7:4>
Color	Single	N/A	Whole	L_DD<7:0>

Table 3-1. LCD Controller Data Pin Utilization (Sheet 2 of 2)

Color/ Monochrome Panel	Single/ Dual Panel	Double-Pixel Mode	Screen Portion	Pins
Color	Dual	N/A	Top	L_DD<7:0>
			Bottom	L_DD<15:8>

NOTE: 1. Double pixel data mode (DPD)=1.

For passive displays, the pins described in Table 3-2 are required connections between the processor and your LCD panel.

Table 3-2. Passive Display Pins Required

Processor Pin	LCD Panel Pin	Pin Type ¹	Definition
L_DD	DU_x, DL_x	Output	Data lines used to transmit either four or eight data values at a time to the LCD display. For monochrome displays, each pin value represents a single pixel; for passive color, groupings of three pin values represent one pixel (red, green, and blue data values). Either the bottom four pins (L_DD<3:0>), the bottom 8 pins (L_DD<7:0>) or all 16 pixel data pins (L_DD<15:0>) will be used as shown in Table 3-1
L_PCLK	Pixel_Clock	Output	Pixel Clock - used by the LCD display to clock the pixel data into the line shift register.
L_LCLK	Line_Clock	Output	Line Clock - used by the LCD display to signal the end of a line of pixels that transfers the line data from the shift register to the screen and increment the line pointers.
L_FCLK	Frame_Clock	Output	Frame Clock - used by the LCD displays to signal the start of a new frame of pixels that resets the line pointers to the top of the screen.
L_BIAS	Bias	Output	AC bias used to signal the LCD display to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset.
N/A	Vcon ²	N/A	Contrast Voltage - Adjustable voltage input to LCD panel - external voltage circuitry is required (no pin available on the processor).

NOTES:

1. "Pin Type" is in reference to the processor. Therefore, outputs are pins that drive a signal from the processor to another device.
2. Vcon is a signal external to the processor. Please refer to "Contrast Voltage" on page 8

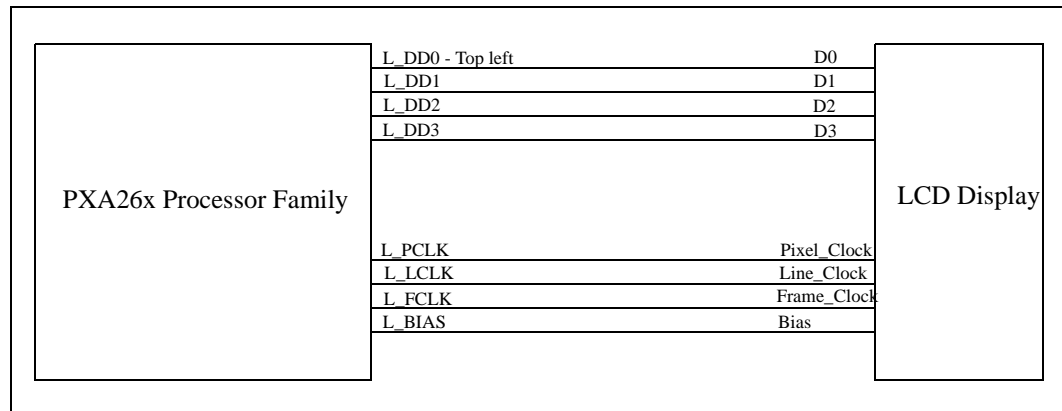
3.2.1 Typical Connections for Passive Panel Displays

The following diagrams are typical connections and serve a guide for designing systems which contain passive LCD displays. Panels differ on which is the panel's least significant bit (refer to the LCD panel reference documentation for the least significant bit). Each figure indicates the top-left pixel (1,1) bit. While dual panels indicates the top-left pixel (1,n/2) of the upper and lower panels and color passive panels show the top-left-pixel color bits.

3.2.1.1 Passive Monochrome Single Panel Displays

Figure 3-1 is a typical single-panel-monochrome passive display connection.

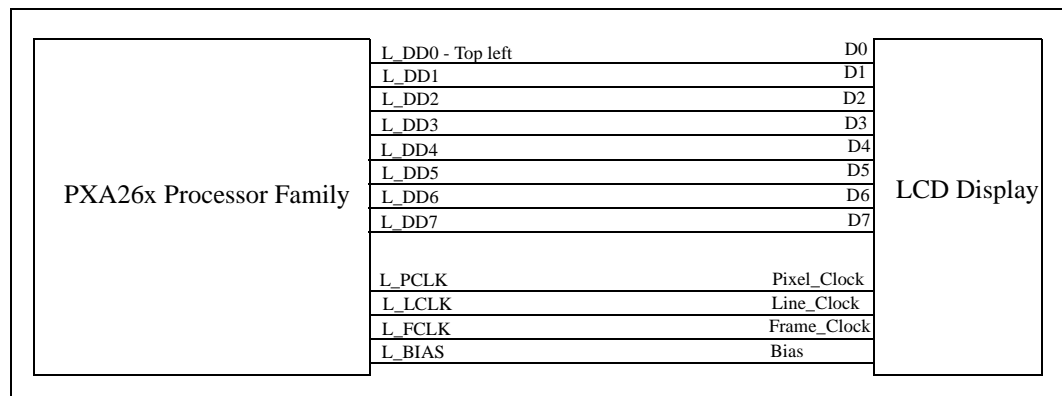
Figure 3-1. Single Panel Monochrome Passive Display Typical Connection



3.2.1.2 Passive Monochrome Single Panel Displays, Double-Pixel Data

Figure 3-2 shows typical connections for a single-panel-monochrome passive display using double-pixel data mode.

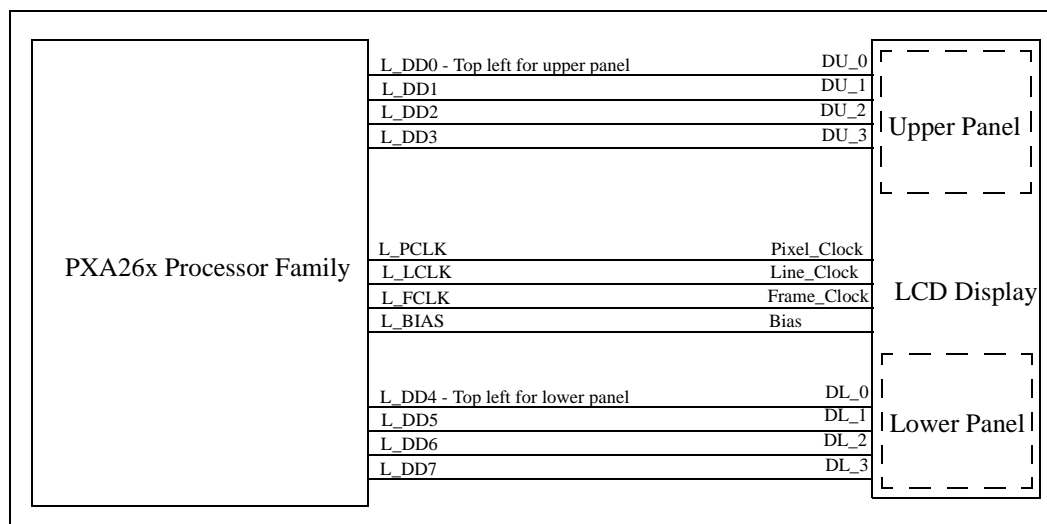
Figure 3-2. Passive Monochrome Single Panel Displays, Double-Pixel Data Typical Connection



3.2.1.3 Passive Monochrome Dual Panel Displays

Figure 3-3 is a typical dual-panel-monochrome passive display connection.

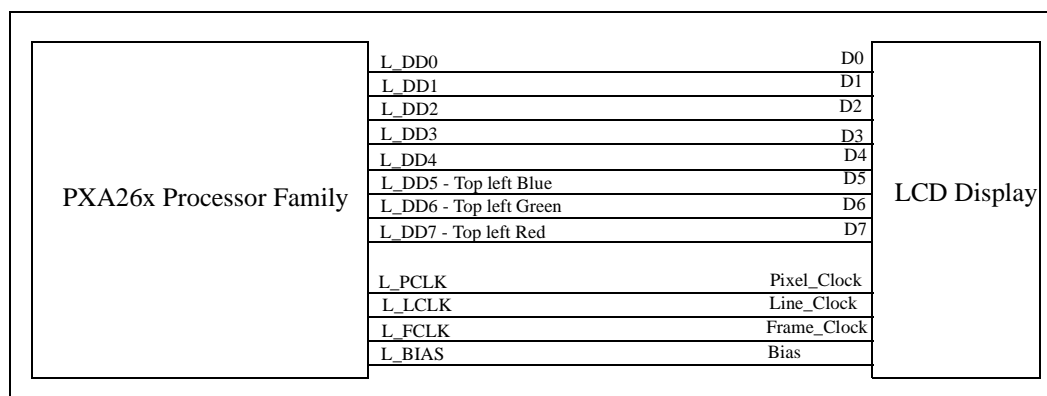
Figure 3-3. Passive Monochrome Dual Panel Displays Typical Connection



3.2.1.4 Passive Color Single Panel Displays

Figure 3-4 is a typical single-panel-color passive display connection.

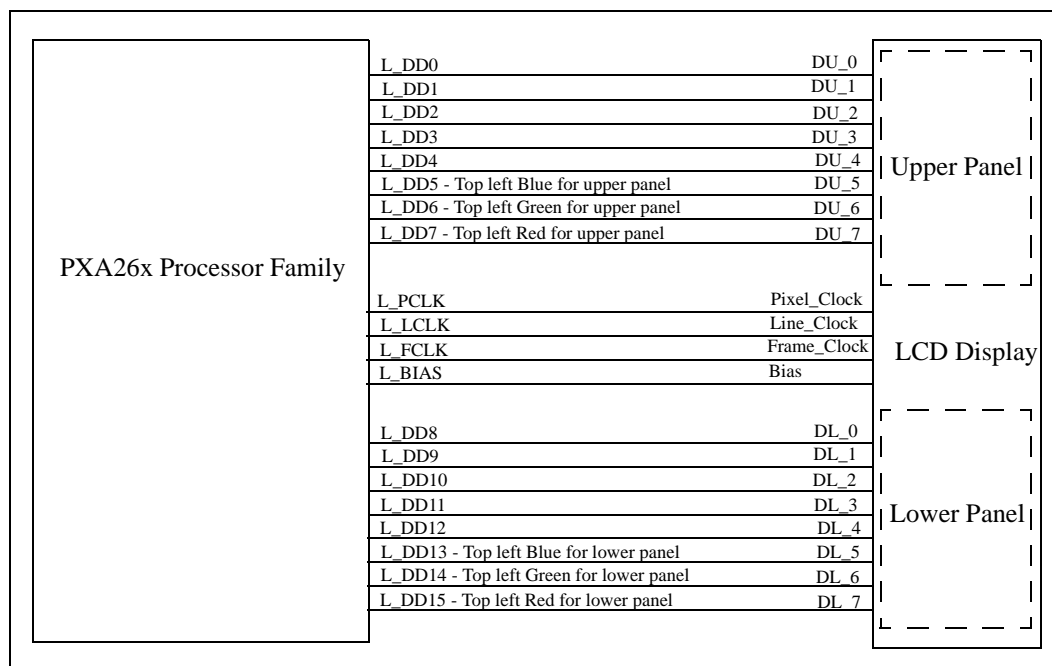
Figure 3-4. Passive Color Single Panel Displays Typical Connection



3.2.1.5 Passive Color Dual Panel Displays

Figure 3-5 is a typical dual-panel-color passive display connection.

Figure 3-5. Passive Color Dual Panel Displays Typical Connection



3.3 Active (TFT) Displays

Because data is sent to the panel as raw 16-bit pixel data, active displays require 16 data pins in order to transfer the pixel data from the controller. All 16 data lines are also required to drive one pixel value. The 16 bits of data describe the intensity level of the red, green and blue for each pixel. Typically, this is formatted as 5-bits for red, 6-bits for green and 5-bits for blue, but this can vary by display and is controlled by the software writing to the frame buffer. Refer to the display datasheet to ensure that the correct processor LCD data lines are connected to the correct LCD panel data lines.

Many active displays actually have more than 16 data lines - usually 18 (6 of each color). For these panels it is recommended that the most significant lines of the panel lines are connected to the data lines from the processor. This maintains the panel's full range of colors but increases the granularity of the color spectrum with an insufficient number of data lines. All unused panel data lines can be tied either high or low. Other options include tying the LSB of red and blue to the next bit, R1 or B1.

For active displays, connect the pins described in Table 3-3 between the processor and the LCD panel.

Table 3-3. Active Display Pins Required

Processor Pin	LCD Panel Pin	Pin Type ¹	Definition
L_DD<15:0>	R<4:0>,G<5:0>,B<4:0>	Output	Data lines used to transmit the 16-bit data values to the LCD display.
L_PCLK	Clock	Output	Pixel clock – used by the LCD display to clock the pixel data into the line shift register. In active mode this clock transitions constantly.
L_LCLK	Horizontal Sync	Output	Line clock – used by the LCD display to signal the end of a line of pixels that transfers the line data from the shift register to the screen and increment the line pointers. Also signals the panel to start a new line.
L_FCLK	Vertical Sync	Output	Frame clock – used by the LCD displays to signal the start of a new frame of pixels that resets the line pointers to the top of the screen.
L_BIAS	DE (Data Enable)	Output	AC biases used in active mode as a data enable signal when data should be latched by the pixel clock from the data lines.
N/A	Vcon ²	N/A	Contrast voltage – Adjustable voltage input to LCD panel - external voltage circuitry is required (no pin available on the processor).

NOTES:

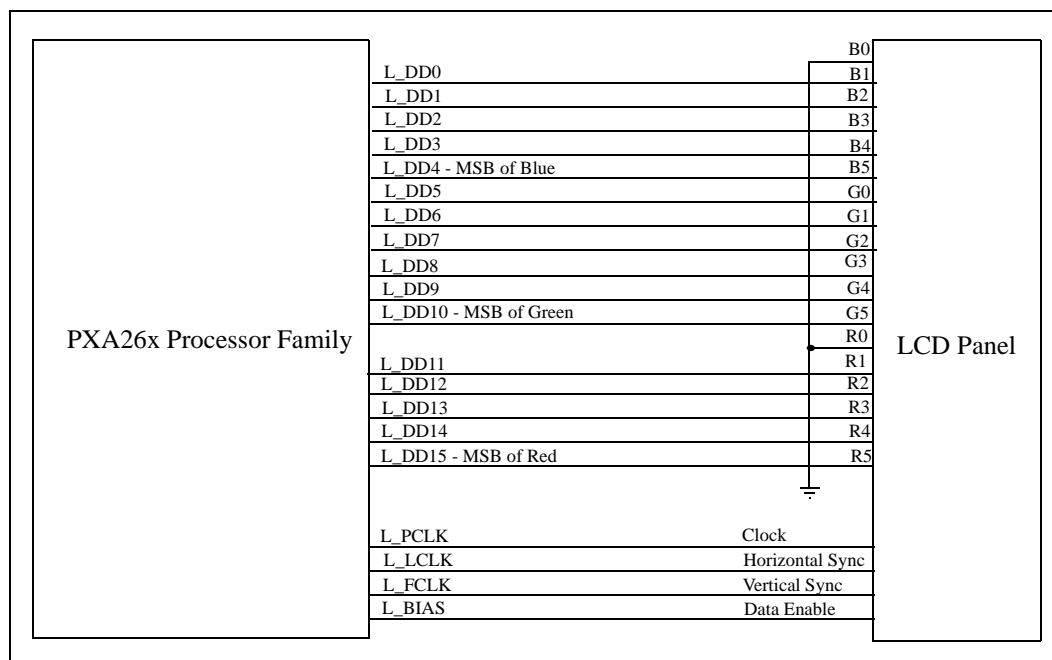
1. In reference to the PXA26x processor family. Therefore, outputs are pins that drive a signal from the processor to another device.
2. Vcon is a signal external to the processor. Please refer to Section 3.5.1.

3.3.1 Typical connections for Active Panel Displays

Figure 3-6 shows a typical connection for an active panel display and should serve as a guide for designing systems which contain active LCD displays. The MSB of each color is indicated. The panel is 18-bit, with the LSB of red and blue tied to ground.

Note: This example shows 6 red, 6 green and 6 blue bits on the LCD panel. However, different active display panels might have more or different data lines. Consult the LCD panel manufacturer's datasheet for the actual data lines.

Figure 3-6. Active Color Display Typical Connection



3.4 Intel® PXA26x Processor Family Pinout

Table 3-4 describes the ball positions for the LCD controller on the processor.

Table 3-4. Intel® PXA26x Processor Family LCD Controller Ball Positions (Sheet 1 of 2)

Pin Name	Ball Position
L_DD0	E7
L_DD1	D7
L_DD2	C7
L_DD3	B7
L_DD4	E6
L_DD5	D6
L_DD6	E5
L_DD7	A6
L_DD8	C5
L_DD9	A5
L_DD10	D5
L_DD11	A4
L_DD12	A3

Table 3-4. Intel® PXA26x Processor Family LCD Controller Ball Positions (Sheet 2 of 2)

Pin Name	Ball Position
L_DD13	A2
L_DD14	C3
L_DD15	B3
L_FCLK	E8
L_LCLK	D8
L_PCLK	B8
Bias	A8

3.5 Additional Design Considerations

3.5.1 Contrast Voltage

Many displays, both active and passive, include a pin for adjusting the display contrast voltage. This is a variable analog voltage that is supplied to the panel via an voltage source on the system board. The contrast voltage is adjusted via a variable resistor on the circuit board.

The required voltage range and current capabilities vary between panel manufacturers. Consult the datasheet for your panel to determine the variable voltage circuit design. Ensure that the contrast voltage is stable, otherwise visual artifacts might result. Possible contrast-voltage circuits are often suggested by the panel manufacturers.

3.5.2 Backlight Inverter

One potential source of noise for the LCD panel can be the backlight inverter. Since this is a high voltage device with frequent voltage inversions, it has the potential to inject spurious noise onto the LCD panel lines. To minimize noise:

- Use a shielded backlight inverter
- Physically locate the inverter as far away from the LCD data lines and system board as possible, usually located with the LCD panel

If power consumption is an issue, chose a backlight inverter that can be disabled through software. This lets you save power by automatically disabling the backlight if no activity occurs within a preset period of time

3.5.3 Signal Routing and Buffering

Signal transmission rates between the LCD controller and the LCD panel are moderate, which helps to simplify the design of the LCD system. The minimum Pixel Clock Divider (PCD) value results in a pixel clock rate of one half of the LCLK (this is not the L_LCLK of the LCD controller). The maximum LCLK for the processor is 148 MHz, resulting in a maximum pixel clock rate of 74 MHz. Thus, use of 100 MHz design considerations are sufficient to ensure LCD panel signal integrity.

However, typical transfer rates are considerably less than 74 Mhz. For example, an 800 x 600 color active display running at 75 Hz requires a transfer rate of approximately 36 MHz. To determine this, calculate the number of pixels ($800 \times 600 = 480,000$) and multiply by the screen refresh rate (75 Hz). Since active panels replace 1 pixel of data with every clock cycle this determines the final transfer rate. Active displays normally do not require refresh rates as high as 75 Hz, so you may use a lower refresh rate to reduce transmission rates even more.

Passive displays often do require refresh rates greater than 75 Hz, which transfers more pixels each clock cycle. For instance, a color passive display with 8 data lines transfers $2 \frac{2}{3}$ pixels' worth of data each clock cycle. This divides the transmission rate by $2 \frac{2}{3}$. Further reductions in the transfer rate come by using dual panel displays which use twice as many data lines to transfer data - halving the rate again.

Generally, this gives you lower transfer rates to even large displays and thus simpler design considerations and fewer layout constraints.

When laying out your design, minimize trace length of the LCD panel signals and allow sufficient spacing between signals to avoid crosstalk. Crosstalk decreases the signal integrity, especially the data line signals.

LCD system design is not considered to be critical as infrequent or single bit errors are, typically, not noticed by the user. Also, the errors are transitory, as the old data is constantly being replaced with new data. Slower panel refresh rates increase the likelihood that a single error is noticed by the user. However, there is a counteracting effect in that slower refresh rates relax LCD timing and therefore result in fewer screen transmission errors. There are other factors related to choosing a refresh rate for an LCD system, most significant is the impact on system bandwidth.

If you must use excessively long or poorly routed signals, one possible solution is to add buffers between the processor and the LCD panel. This helps strengthen the LCD panel signal levels and synchronizes signal timing. However, this is usually not required as the LCD panel timings are fairly relaxed. Since the LCD display essentially operates asynchronously from the processor, the propagation delay of the buffers is not a major concern.

When mounting the LCD panel, it is critical to shield any touchscreen control lines that may be present. Noise from the LCD panel and its control signals can become injected into the touchscreen control lines, causing spurious touch interrupts or loss of resolution.

3.5.4 Panel Connector

Most LCD panels are connected to the system board via a connector, instead of being directly mounted on the system board. This increases flexibility and ease of manufacture. Typically the manufacturer of the panel recommends a particular connector for the panel. Follow the panel manufacturer's recommendation.

4.1 Self Powered Device

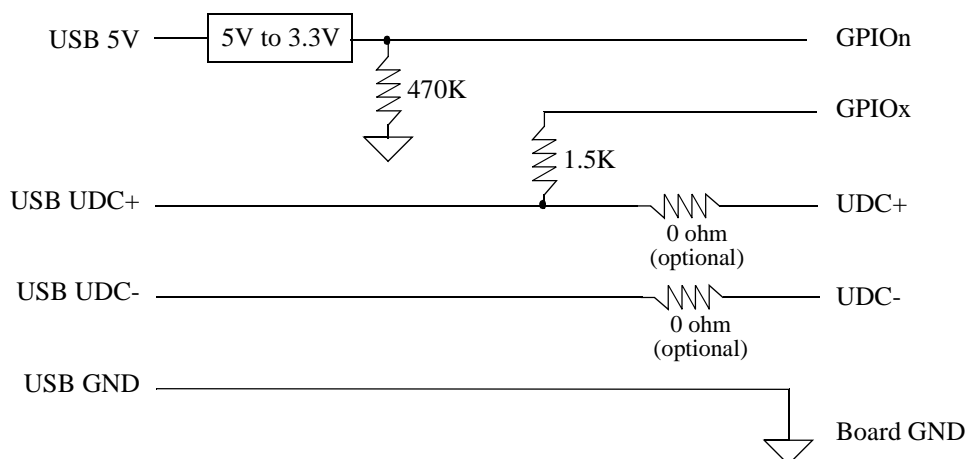
Figure 4-1 shows the USB interface connection for a self-powered device. If not using the optional 0 ohm resistors connect USB UDC+ directly to the device UDC+ and connect USB UDC- directly to device UDC-. The device UDC+ and UDC- pins match the impedance of a USB cable, 90 ohms, without the use of external series resistors. You may install 0 ohm resistors on your board to compensate for minor differences between the USB cable and your board trace impedance.

The 5 to 3.3 voltage divider is required because the device GPIO pins cannot exceed 3.3 V. This voltage divider can be implemented in a number of ways. The most robust and expensive solution is to use a Maxim* MAX6348 Power-On-Reset device. This solution produces a very clean signal edge and minimizes signal bounce. The less expensive solution is to use a 3.3 V line buffer with 5 V tolerant inputs. This solution does not reduce signal bounce, so software must compensate by reading the GPIO signal after it stabilizes. A third solution is to implement a signal bounce minimization circuit that is 5 V tolerant, but produces a 3.3 V signal to the GPIO pin.

Note: If GPIO_n and GPIO_x are the same pin, never put the device to sleep while the USB cable is connected to the device. During sleep, the USB controller is in reset and does not respond to the host; after sleep, the device does not respond to its host-assigned address.

Note: VCCQ must be 3.3 V \pm 10% for proper operation of the differential pins.

Figure 4-1. Self Powered Device



4.1.1 Operation if GPIOn and GPIOx are Different Pins

Any GPIO pins can be defined as GPIOn and GPIOx. GPIOn should be a GPIO which can bring the device out of sleep. Out of reset, configure GPIOx as an input that causes the UDC+ line to float. GPIOn is configured as an input that causes an interrupt whenever a rising or falling edge is detected. When an interrupt occurs, software must read the GPIOn pin to determine if the cable is connected or not. GPIOn is 1 if the cable is connected or 0 if the cable is disconnected. If a USB connect is detected, software enables the UDC peripheral and drives a 1 onto the GPIOx pin to indicate to the host PC a fast USB device is connected. If a USB disconnect is detected, software must configure the GPIOx pin as an input, configure the GPIOn pin to detect a wakeup event, and then put the part into sleep mode.

Also, at any time, you can use software to put the part into sleep mode. Before entering sleep mode, configure the GPIOx pin as an input to cause the UDC+ line to float. This looks like a disconnect to the host PC. The device can then be put into sleep mode. When the device becomes active, software must drive a 1 onto the GPIOx pin to indicate to the host PC a fast USB device has been connected.

4.1.2 Operation if GPIOn and GPIOx are the Same Pin

Out of reset, GPIOn is configured as an input and configured to cause an interrupt whenever a rising or falling edge is detected. When an interrupt occurs, software must read the GPIOn pin to determine if the cable is connected or not. This pin is 1 if the cable is connected or 0 if the cable is disconnected. If the USB cable is connected, then software must enable the UDC peripheral before the host sends the first USB command. If the USB cable is not connected, then software must configure the GPIOn pin to detect a wakeup event, and then put the part into sleep mode.

4.2 Bus Powered Device

The Intel® PXA26x Processor Family cannot support a bus powered device model. When the host sends a suspend, the device is required to consume less than 500 μ A (Section 7.2.3 of the *USB Specification version 1.1*). The processor cannot limit its current consumption to 500 μ A unless it enters sleep mode. If it enters sleep mode, all USB registers are reset and it does not respond to its host-assigned address.

4.3 Single-Ended USB connection

The processor adds support for a 6-pin interface compatible with the Philips Semiconductors* PDIUSBP11A transceiver with the MODE pin grounded and SPEED pin driven high. Suspend is not supported with this interface, and if needed must be implemented with a separate GPIO. Two of the pins are multiplexed with the FFUART, which simplifies the physical interface for synchronization by allowing software to automatically choose between a USB or UART interface.

To enable the 6-pin interface, the GPIO pins associated with it must be set to the appropriate alternate function. When all the pins in the interface are enabled, the default USB interface pins, USB_P and USB_N are automatically disabled. USB_P and USB_N must be driven to ground when using the 6-pin interface. Figure 4-2 shows how to connect the single-ended interface to the PDIUSBP11A.

Figure 4-2. Single-Ended USB connection


The MultiMediaCard (MMC) is a low cost data storage and communication medium. The MMC supports the translation protocol from a standard MMC or Serial Peripheral Interface (SPI) bus to an application bus.

The MMC controller in the processor is compliant with *The MultiMediaCard System Specification, Version 2.1*. The only exception is one and three byte data transfers are not supported. The MMC controller is capable of communicating with a card in MMC or SPI mode. Your application is responsible for specifying the MMC controller communication mode.

5.1 Schematics

The MultiMediaCard (MMC) controller on the processor supports MMC and SDCard devices. (The MMC controller does not support SDCard nibble mode.) This section presents several options for connecting each type of device to the controller.

5.1.1 Signal Description

MMC controller signal functions are described in Table 5-1.

Table 5-1. MMC Signal Description

Signal Name	Input/Output	Description
MMCLK	Output	Clock signal to MMC
MMCMD	Bi-directional	Command line
MMDAT	Bi-directional	Data line
MMCCS0	Output	Chip Select 0
MMCCS1	Output	Chip Select 1

The MMCLK, MMCCS0, and MMCCS1 signals are routed through alternate functions within the processor general purpose input/output (GPIO) module. Each of these signals can be programmed to a particular GPIO pin.

The signals defined in *The MultiMediaCard System Specification* for an MMC device are CLK, CMD, and DAT which correspond to the MMCLK, MMCMD, and MMDAT in the processor, respectively. The two chip selects in the controller are for the MMC SPI mode and correspond to the reserved pin of two different devices, defined in the specification.

The signals defined in the *Physical Layer Specification* of the *SD Memory Card Specifications* for an SDCard device are CLK, CMD, and DAT0-DAT3. The obvious difference is the number of DAT signals. In addition, the socket for an SDCard contains mechanical switches for write protect (WP) and card detect (CD). For an SDCard to be connected to the MMC controller, only one data line, DAT0, is used. Otherwise, the signal mapping remains the same as an MMC device. The WP and CD switches on the socket are discussed in Section 5.1.2.

5.1.2 How to Wire

Note: The example schematic in Figure 5-1 uses an SDCard socket. The signals on the socket are defined in Table 5-2.

Table 5-2. SDCard Socket Signals

Signal Name	Pin #
DAT3	1
CMD	2
VSS1	3
VDD	4
CLK	5
VSS2	6
DAT0	7
DAT1	8
DAT2	9

As stated previously, the Intel® PXA26x Processor Family MMC controller can be connected to either an MMC device or an SDCard device, but you are limited to which device installs in which socket. Refer to Table 5-3 for information on sockets and device supported by the MMC controller.

Table 5-3. MMC Controller Supported Sockets and Devices

Sockets	Devices Supported
SDCard socket	SDCard device MMC device
MMC socket	MMC device

Figure 5-1 is a schematic that supports both MMC and SDCard devices. In the schematic, the signals SA_MMCLK, SA_MMCMMD, and SA_DAT correspond to the processor signals MMCLK, MMCMMD, and MMDAT, respectively. These three signals are also directly connected to the socket.

Three other signals shown on the connector are COMM and the mechanical switches, WP and CD. Both WP and CD connect to COMM via a mechanical switch inside the socket when a device is inserted.

Three other signals shown on the connector are COMM and the mechanical switches WP and CD. When a device is inserted in the example schematic (Figure 5-1), WP may be and CD is connected to COMM via a mechanical switch inside the socket

SDCard devices have a write protect tab. Depending on the position of the tab, the WP signal may or may not be connected to the COMM signal. Connect the WP signal to a CPLD or other device capable of indicating to the driver software that the card is write protected. In this example, COMM is tied to VCC and WP has a pull-down resistor. This causes a rising edge when the tab is in the write protect position and the WP signal remains low when the tab is in the read/write position.

The CD signal, MMC_DETECT, indicates to the MMC controller when a card is installed. It is used for both an SDCard socket and an MMC socket. Since the MMC socket does not have the mechanical CD switch, other measures must be taken to produce a card detect.

Note: While this schematic shows two ways to create a card detect, it is recommended that an SDCard socket be used if a card detect and write protection signal are desired even if only MMC devices are being used.

5.1.2.1 SDCard Socket

When using Figure 5-1 as a template for your SDCard circuit design, all resistors labeled “DNI IF SD” should not be installed and all resistors labeled “DNI IF MMC” should be installed in the circuit. Removing R226 and inserting R225 causes the VSS2 signal on pin 6 to be tied to ground. Also, the SDCard needs a pull-down resistor in position R228.

SDCard sockets have a card detect switch internal to the socket. The CD signal is physically connected to the COMM signal. Connect the CD signal to a CPLD or other device capable of indicating to the driver software that a card has been inserted in the socket. In this example, COMM is tied to a V_{CC} and CD has a pull-down resistor. This causes a rising edge on CD when a card is inserted while the CD signal remains low if no card is in the socket.

5.1.2.2 MMC Socket

When using Figure 5-1 as a template for your MMC circuit design, all resistors labeled “DNI IF MMC” should not be installed and all resistors labeled “DNI IF SD” should be installed in the circuit. This causes the VSS2 signal on pin 6 to be pulled-up through resistor R227.

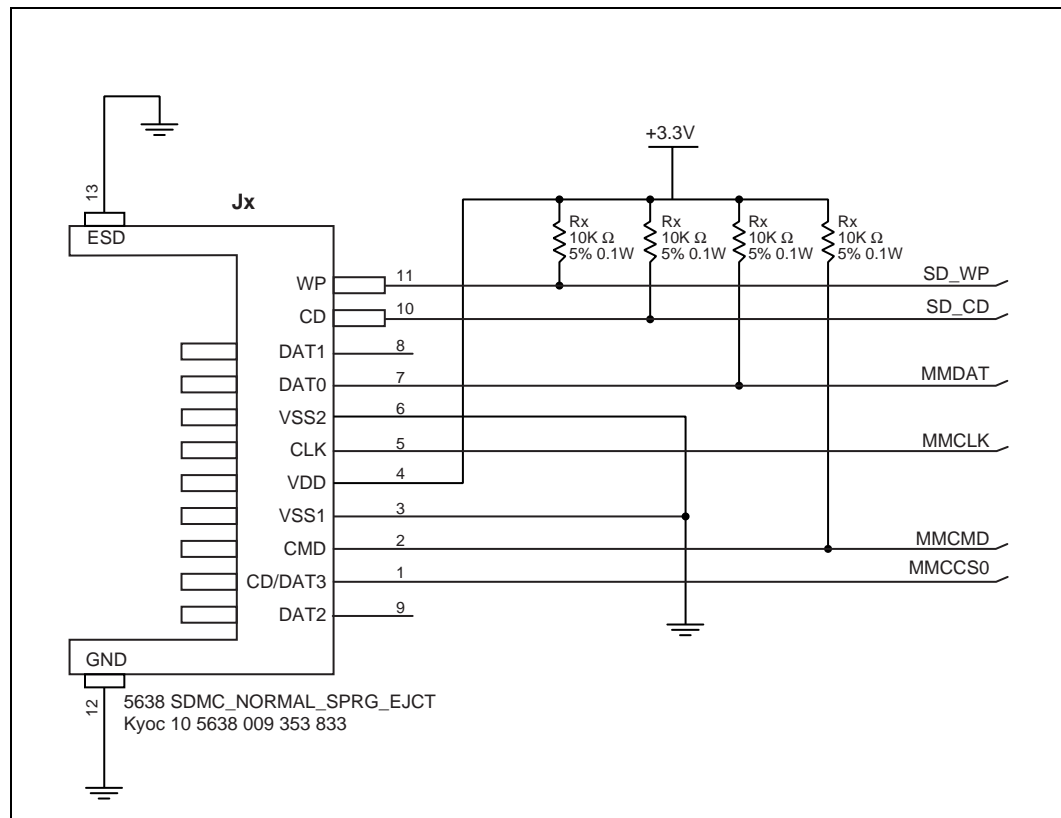
Unlike SDCard sockets, MMC sockets do not have a CD or WP switch. In order to implement this, a pull-up is placed on the VSS2 signal (pin 6 of the socket.) Since VSS2 and VSS1 are connected internally on the MMC device, the signal called nMMC_DETECT on the schematic is driven low when the MMC device is inserted.

Warning: Connecting VSS2 to something other than the power supply ground violates *The MultiMediaCard System Specification, Version 2.1*. Because the MMC specification does not state that VSS1 and VSS2 must be connected internal to the MMC device, the design in Figure 5-1 may not work with all MMC devices. Use caution when using the card detection method shown in Figure 5-1.

5.1.3 Simplified Schematic

Figure 5-2 shows another SDCard socket. In this case, all processor signals are connected to the socket. This socket does not have a common signal for the write protect and card detect and are connected to the two tabs shown on the left side of the diagram. Inserting a card into the socket may cause the write protect signal and will cause the card detect signal to change states and must be interpreted by the CPLD software.

Figure 5-2. Processor MMC to SDCard Simplified Signal Connection



5.1.4 Pull-up and Pull-down

Table 5-4 and Table 5-5 show the pull-up and pull-down resistors required for SDCard and MMC devices according to their respective specifications.

Table 5-4. SDCard Pull-up and Pull-down Resistors

Signal	Pull-up or Pull-down	Min	Max	Remark
CMD	pull-up	10 k Ω	100 k Ω	Prevents bus floating
DAT0-DAT3	pull-up	10 k Ω	100 k Ω	Prevents bus floating
WP ¹	pull-up	—	—	Any value sufficient to prevent bus floating
NOTE: 1. This resistor is shown in the specification but the value is not specified				

Table 5-5. MMC Pull-up and Pull-down Resistors

Signal	Pull-up or Pull-down	Min	Max	Remark
CMD	pull-up	4.7 k Ω	100 k Ω	Prevents bus floating
DAT	pull-up	50 k Ω	100 k Ω	Prevents bus floating

5.2 Utilized Features

The processor MultiMediaCard controller has these features:

- Data transfer rates as fast as 20 Mbps
- A 16-bit response FIFO
- Dual receive data FIFOs
- Dual transmit FIFOs
- Support for two MMCs in either MMC or SPI mode

The sample schematics in this chapter support MMC and SDCard and are configured to use MMC or SPI mode.

The processor's MMC controller and the MMC device have the same maximum data rate, 20 Mbps, so their communication rates are compatible. However, because the maximum processor MultiMediaCard controller data rate is 20 Mbps and the maximum SDCard data rate is 25 Mbps, SDCard devices are not utilized to their fullest extent.

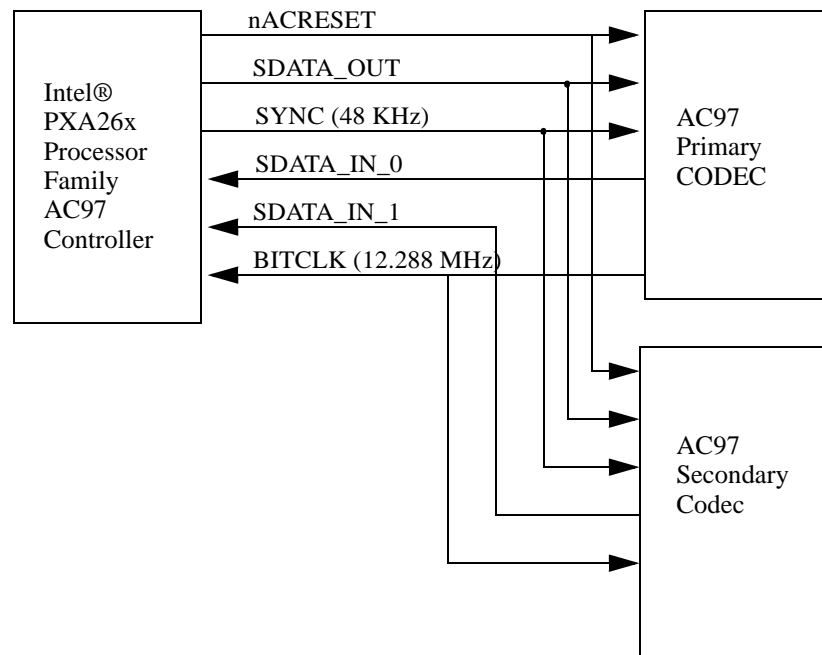
The circuit designs presented in this chapter (Figure 5-1 and Figure 5-2) only show support for one SDCard or MMC device, but the processor's MMC controller can handle as many as two devices.

The AC97 controller unit (ACUNIT) connects audio chips and codecs to the processor. It uses a six-wire interface to transmit and receive data from AC97 2.0 compliant codecs. The AC97 port is a bi-directional, serial PCM digital stream. A maximum of two codecs may be connected to the ACUNIT.

6.1 Schematics

The schematics for an AC97 connection are shown in Figure 6-1. The primary codec supplies the 12.288 MHz clock to the AC97. This clock is then driven into the ACUNIT on the processor and the AC97 Secondary Codec.

Figure 6-1. AC97 connection



6.2 Layout

Because of the analog/digital nature of the AC97 Codecs, it is important that proper mixed-signal layout procedures be followed. Intel recommends you follow the layout recommendations given in your Codec datasheet. Some general recommendations are:

- Use a separate power supply for the analog audio portion of the design.
- Place a digital power/ground plane keep-out underneath the analog portion. Use a separate analog ground plane. You can create an island inside the keep-out. Connect the digital ground pins of the codec to the digital ground. Keep the two ground planes on the same layer, with at least 1/8 of an inch separation between them.
- Connect the two ground planes underneath your codec with a 0 ohm jumper. Add optional do not populate 0 ohm jumpers between analog and digital ground at the power supply. Excessive noise on the board may be reduced by installing the 0 ohm resistor.
- Do not route digital signals underneath the analog portion. Digital traces must go over the digital ground plane, analog traces over the analog plane.
- Buffer any digital signals to or from the codec that go off the board, for example, if your codec is on a daughter card.
- Fill the areas between analog traces with copper tied to the analog ground. Fill the regions between digital traces with copper tied to the digital ground.
- Locate the decoupling capacitors for the analog portion as close to the codec as possible.

The Inter-Integrated Circuit (I²C) bus interface unit lets the processor serve as a master and slave device residing on the I²C bus. The I²C bus is a serial bus developed by Philips Corporation consisting of a two-pin interface. SDA is the serial data line and SCL is the serial clock line.

Using the I²C bus lets the processor interface with other I²C peripherals and microcontrollers for system management functions. The serial bus requires a minimum of hardware for an economical system to relay status and reliability information to an external device.

The I²C bus interface unit is a peripheral device that resides on the processor internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to the I²C Bus Specification for complete details on I²C bus operation.

7.1 Schematics

Many different applications use the I²C bus. This chapter presents two possible methods for using the I²C bus interface. The first method controls a digital-to-analog converter (DAC) to vary the DC voltage to the processor core. The second method expands the capabilities of an existing compact flash socket.

7.1.1 Signal Description

The I²C bus interface unit signals are SDA and SCL. Table 7-1 describes the function of each signal.

Table 7-1. I²C Signal Description

Signal Name	Input/Output	Description
SDA	Bi-directional	Serial data
SCL	Bi-directional	Serial clock

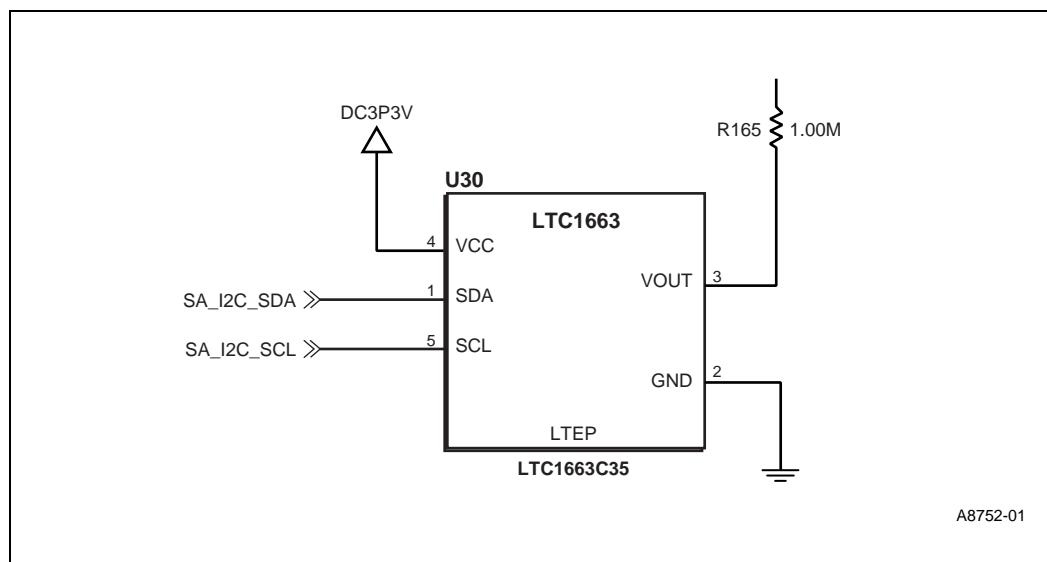
The I²C bus serial operation uses an open-drain, wired-AND bus structure, which allows multiple devices to drive the bus lines and to communicate status about events such as arbitration, wait states, error conditions and so on. For example, when a master drives the clock (SCL) line during a data transfer, it transfers a bit on every instance that the clock is high. When the slave is unable to accept or drive data at the rate that the master is requesting, the slave can hold the clock line low between the high states to insert a wait interval. The master's clock can only be altered by a slow slave peripheral keeping the clock line low or by another master during arbitration.

The I²C bus lets you design a multi-master system; meaning more than one device can initiate data transfers at the same time. To support this feature, the I²C bus arbitration relies on the wired-AND connection of all I²C interfaces to the I²C bus. Two masters can drive the bus simultaneously provided they are driving identical data. The first master to drive SDA high while another master drives SDA low loses the arbitration. The SCL line consists of a synchronized combination of clocks generated by the masters using the wired-AND connection to the SCL line.

7.1.2 Digital-to-Analog Converter (DAC)

Figure 7-1 shows the schematic for connecting the I²C interface to a Linear Technology micropower DAC. The DAC output is connected to the buck converter feedback path and is controlled by the I²C bus interface unit. The DAC can modify the voltage of the feedback path, which effects the processor core voltage.

Figure 7-1. Linear Technology DAC with I²C Interface



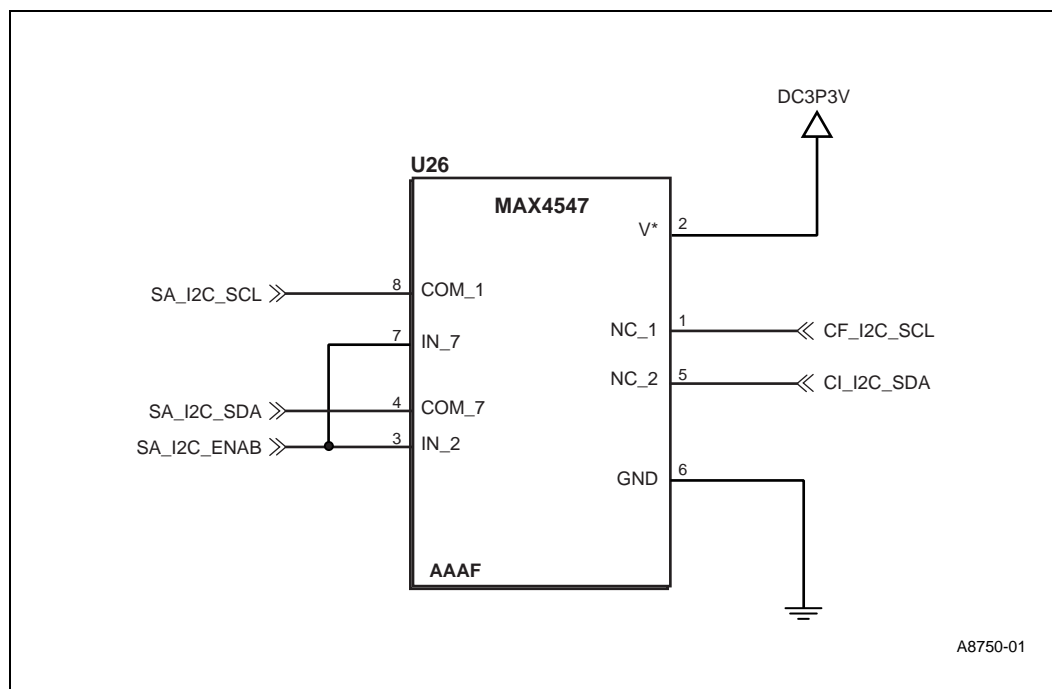
The signals, SA_I2C_SDA and SA_I2C_SCL, correspond to the processor signals SDA and SCL, respectively.

7.1.3 Other Uses of I²C

Figure 7-2 shows the I²C signals passing through an analog switch to a compact flash socket. Because the CF socket has all of the signals to support two CF cards, and this design only uses one CF card, the signals meant for a second card are being used for alternate functions. If you decide not to use a CF card, a different application using a CF card socket could be designed to utilize the I²C bus interface unit. If this alternate function is used, the I²C bus can be enabled to bypass the CF socket by asserting the signal SA_I2C_ENAB shown in the diagram. If the user decides to use a CF Card, negate the SA_I2C_ENAB signal so the I²C bus traffic does not interfere with the CF card.

Note: The CF card socket is disabled if a device is inserted into the expansion bus.

Figure 7-2. Using an Analog Switch to Allow a Second CF Card



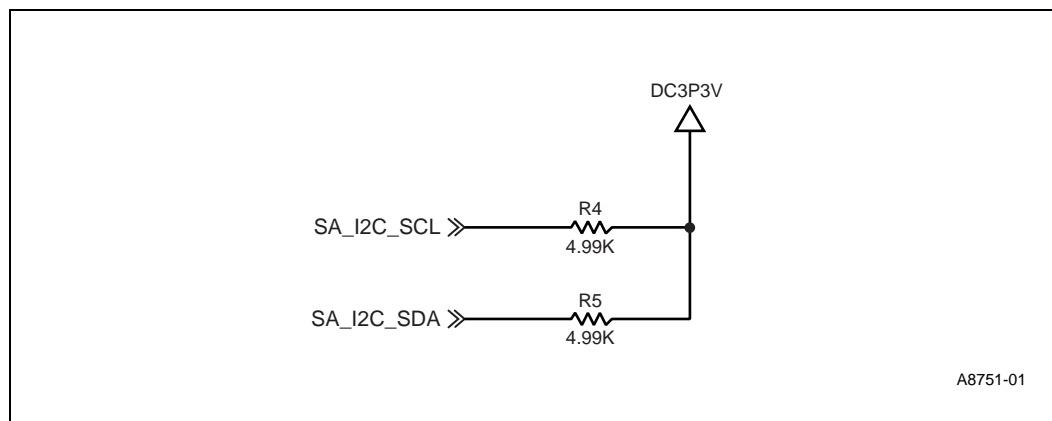
7.1.4 Pull-Ups and Pull-Downs

The *I²C Bus Specification*, available from Philips Corporation, states:

The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I2C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit.

The design presented in chapter is not intended for loads larger than 200 pF, so the pull-up device is a resistor as shown in Figure 7-3.

Figure 7-3. I²C Pull-Ups and Pull-Downs



The actual value of the pull-up is system dependant and a guide is presented in the *I²C Bus Specification* on determining the maximum and minimum resistors to use when the system is intended for standard or fast-mode I²C bus devices.

7.2 Utilized Features

The processor I²C bus interface unit is compatible with the two pin interface developed by Philips Corporation. A complete list of features and capabilities can be found in the *I²C Bus Specification*.

8.1 Operating Conditions

Table 8-1 shows voltage, frequency, and temperature specifications for the processor for four different ranges. The temperature specification for each range is constant; the frequency range is operation voltage dependent. On a prototype design, the VCC/PLL_VCC regulator should have a range from 0.85 V to 1.65 V. PLL_VCC and VCC must be connected together on the board or driven by the same supply.

Table 8-1. Voltage, Temperature, and Frequency Electrical Specifications

Symbol	Description	Min	Typical	Max
t_A	Ambient Temperature	-40°C	—	85° C
V_{VSS}	VSS, VSSN, VSSQ Voltage	-0.3 V	0 V	0.3 V
V_{VCCQ_H}	VCCQ @ 3.3V	3.0 V	3.3 V	3.6 V
V_{VCCQ_L}	VCCQ @ 2.775V	2.636 V	2.775 V	2.914 V
V_{VCCN_H}	VCCN @ 3.3V	3.0 V	3.3 V	3.6 V
V_{VCCN_M}	VCCN @ 2.775V	2.636 V	2.775 V	2.914 V
V_{VCCN_L}	VCCN @ 2.5V	2.375 V	2.5 V	2.625 V
Low Voltage Range				
V_{VCC_L}	VCC, PLL_VCC Voltage, Low Range	0.8075 V	0.85 V	0.935 V
f_{TURBO_L}	Turbo Mode Frequency, Low Range	99.5 MHz	—	132.7 MHz
f_{SDRAM_L}	External Synchronous Memory Frequency, Low Range	—	—	66.4 MHz
Medium Voltage Range				
V_{VCC_M}	VCC, PLL_VCC Voltage, Mid Range	0.9 V	1.0 V	1.1 V
f_{TURBO_M}	Turbo Mode Frequency, Mid Range	99.5 MHz	—	199.1 MHz
f_{SDRAM_M}	External Synchronous Memory Frequency, Mid Range	—	—	99.5 MHz
High Voltage Range				
V_{VCC_H}	VCC, PLL_VCC Voltage, High Range	1.0 V	1.1 V	1.21 V
f_{TURBO_H}	Turbo Mode Frequency, High Range	99.5 MHz	—	298.7 MHz
f_{SDRAM_H}	External Synchronous Memory Frequency, High Range	—	—	99.5 MHz
NOTE: When VCCN = 2.5 V or 2.775 V, the I/O signals that are supplied by VCCN are 2.5 V or 2.775 V tolerant only. Do not apply 3.3 V to any pin supplied by VCCN in this case.				

8.2 Electrical Specifications

Table 8-2 provides the absolute maximum ratings for the processor. Do not exceed these parameters or the part may be permanently damaged. Operation at absolute maximum ratings is not guaranteed.

Table 8-2. Absolute Maximum Ratings

Symbol	Description	Min	Max
T_S	Storage Temperature	-40° C	125° C
V_{SS_O}	Offset Voltage between any two VSS pins (VSS, VSSQ, VSSN)	-0.3 V	0.3 V
V_{CC_O}	Offset Voltage between any of the following pins: VCCQ, VCCN	-0.3 V	0.3 V
V_{CC_HV}	Voltage Applied to High Voltage Supplies (VCCQ, VCCN)	VSS-0.3 V	VSS+4.0 V
V_{CC_LV}	Voltage Applied to Low Voltage Supplies (VCC, PLL_VCC)	VSS-0.3 V	VSS+1.65 V
V_{IP}	Voltage Applied to non-Supply pins except XTAL pins	VSS-0.3 V	max of VCCQ+0.3 V, VSS+4.0 V
V_{IP_X}	Voltage Applied to XTAL pins (PXTAL, PEXTAL, TXTAL, TEXTAL)	VSS-0.3 V	max of VCC+0.3 V, VSS+1.65 V
V_{ESD}	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000 V
I_{EOS}	Maximum DC Input Current (Electrical Overstress) for any non-supply pin		5 mA

8.3 Oscillator Electrical Specifications

The processor contains two oscillators – 32.768 kHz and 3.6864 MHz; each chosen for a specific crystal. When choosing a crystal, match the crystal parameters as closely as possible.

8.3.1 32.768 kHz Oscillator Specifications

The 32.768 kHz oscillator is connected between the TXTAL (amplifier input) and TEXTAL (amplified output). The 32.768 kHz specifications are shown in Table 8-3.

Table 8-3. 32.768 kHz Oscillator Specifications (Sheet 1 of 2)

Symbol	Description	Min	Typical	Max
Crystal Specifications - Typical is FOX NC38				
F_{XT}	Crystal Frequency, TXTAL/TEXTAL	—	32.768 KHz	—
ESR	Equivalent series resistance, TXTAL/TEXTAL	6 K Ω	—	65 K Ω
P	Drive Level	—	—	1 μ W
Amplifier Specifications				
V_{IH_X}	Input High Voltage, TXTAL	0.8 V*VCC	—	VCC
V_{IL_X}	Input Low Voltage, TXTAL	VSS	—	0.2 V*VCC
I_{IN_XT}	Input Leakage, TXTAL	—	—	1 μ A

Table 8-3. 32.768 kHz Oscillator Specifications (Sheet 2 of 2)

Symbol	Description	Min	Typical	Max
C _{IN_XT}	Input Capacitance, XTAL/TEXTAL	—	18 pF	25 pF
t _{S_XT}	Stabilization Time	2 s	—	10 s
Board Specifications				
R _{P_XT}	Parasitic Resistance, XTAL/TEXTAL to any node	20 MΩ	—	—
C _{P_XT}	Parasitic Capacitance, XTAL/TEXTAL, total	—	—	5 pF
C _{OP_XT}	Parasitic Shunt Capacitance, XTAL to TEXTAL	—	—	0.4 pF

To drive the 32.768 kHz crystal pins from an external source:

- Drive the TEXTAL pin with a digital signal that has a low level near 0 V and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is 1 V per μs. The maximum current drawn by the external clock source when the clock is at its maximum positive voltage should be about 1 mA.
- Float the XTAL pin or drive it complementary to the TEXTAL pin, using the same voltage level, slew rate, and input current restrictions.

8.3.2 3.6864 MHz Oscillator Specifications

The 3.6864 MHz oscillator is connected between the PXTAL (amplifier input) and PEXTAL (amplified output). The 3.6864 MHz specifications are shown in Table 8-4

Table 8-4. 3.6864 MHz Oscillator Specifications

Symbol	Description	Min	Typical	Max
Crystal Specifications - Typical is FOX HC49S				
F _{XP}	Crystal Frequency, PXTAL/PEXTAL	—	3.6864 MHz	—
ESR	Equivalent series resistance, XTAL/TEXTAL	50 Ω	—	300 Ω
P	Drive Level	—	—	100 μW
Amplifier Specifications				
V _{IH_X}	Input High Voltage, PXTAL	0.8V*VCC	—	VCC
V _{IL_X}	Input Low Voltage, PXTAL	VSS	—	0.2 V*VCC
I _{IN_XP}	Input Leakage, PXTAL	—	—	10 μA
C _{IN_XP}	Input Capacitance, PXTAL/PEXTAL	—	40 pF	50 pF
t _{S_XP}	Stabilization Time	17.8 ms	—	67.8 ms
Board Specifications				
R _{P_XP}	Parasitic Resistance, PXTAL/PEXTAL to any node	20 MΩ	—	—
C _{P_XP}	Parasitic Capacitance, PXTAL/PEXTAL, total	—	—	5 pF
C _{OP_XP}	Parasitic Shunt Capacitance, PXTAL to PEXTAL	—	—	0.4 pF

To drive the 3.6864 MHz crystal pins from an external source:

- Drive the PEXTAL pin with a digital signal that has a low level near 0 V and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is

1 V per 100 ns. The maximum current drawn by the external clock source when the clock is at its maximum positive voltage should be about 1 mA.

- Float the PXTAL pin or drive it complementary to the PEXTAL pin, using the same voltage level, slew rate, and input current restrictions. If floated, some degree of noise susceptibility will be introduced in the system, and it is therefore not recommended.
- The minimum duty cycle for an external signal driven into PEXTAL is 40/60.

8.4 Reset and Power AC Timing Specifications

The processor asserts the nRESET_OUT pin in one of several modes:

- Power-on
- Hardware reset
- Watchdog reset
- GPIO reset
- Sleep mode

The following sections give the timing and other specifications for the entry and exit of these modes.

8.4.1 Power Supply Connectivity

The Intel® PXA26x Processor Family requires two or three externally-supplied voltage levels. VCCQ requires 3.3 V or 2.775 V, VCCN requires 3.3 V, 2.775 V or 2.5 V, and VCC and PLL_VCC require a supply of 1.1 V to 0.85 V. PLL_VCC must be the same voltage as VCC. In general, PLL_VCC and VCC should be tied together. Depending on the availability of independent regulator outputs and the desired memory voltage, VCCQ may have to be separated from VCCN. VCCN does not have to be separated at the board level. Table 8-5 shows the differences between VCCN and VCCQ.

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 1 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
MA(25:0)	26	Main Memory Address Bus	VCCN
MD(31:16)	16	Main Memory Data Bus (high)	VCCN
MD(15:0)	16	Main Memory Data Bus (low)	VCCN
nOE	1	Main Memory Bus Output Enable	VCCN
nWE	1	Main Memory Bus Write Enable	VCCN
nSDRAS	1	Main Memory Bus RAS	VCCN
nSDCAS	1	Main Memory Bus CAS	VCCN
DQM(3:2)	2	Main Memory Bus SDRAM byte selects	VCCN
DQM(1:0)	2	Main Memory Bus SDRAM byte selects	VCCN
nSDCS(2)/GP86	1	Main Memory Bus SDRAM chip select	VCCN

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 2 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
nSDCS(3)/GP87	1	Main Memory Bus SDRAM chip select	VCCN
nSDCS(1:0)	2	Main Memory Bus SDRAM chip selects	VCCN
SDCKE(1:0)	2	Main Memory Bus SDRAM clock enable	VCCN
SDCLK(2)	1	Main Memory Bus SDRAM clocks	VCCN
SDCLK(1:0)	2	Main Memory Bus SDRAM clocks	VCCN
RD/nWR/GP88	1	CC Steering Signal	VCCN
CS(0)	1	Static chip selects	VCCN
GP15	1	Active low chip select 1	VCCN
GP18	1	Ext. Bus Ready	VCCN
GP19	1	Ext. Bus Master Request	VCCN
GP20	1	Ext. Bus Master Request	VCCN
GP21	1	General Purpose I/O pin	VCCN
GP22	1	General Purpose I/O pin	VCCN
GP33	1	Active low chip select 5	VCCN
GP48	1	Output Enable for Card Space	VCCN
GP49	1	Write Enable for Card Space	VCCN
GP50	1	I/O Read for Card Space	VCCN
GP51	1	I/O Write for Card Space	VCCN
GP52	1	Card Enable for Card Space	VCCN
GP53	1	Card Enable for Card Space	VCCN
		MMC CLock	
GP54	1	MMC CLock	VCCN
		Socket Select for Card Space	
GP55	1	Card Address bit 26	VCCN
GP56	1	Wait signal for Card Space	VCCN
GP57	1	Bus Width select for I/O Card Space	VCCN
GP78	1	Active low chip select 2	VCCN
GP79	1	Active low chip select 3	VCCN
GP80	1	Active low chip select 4	VCCN
MMCMD	1	MMC Command	VCCQ
MMDAT	1	MMC Data	VCCQ
nACRESET/GP89	1	AC97 RESET	VCCQ
UDC+	1	USB client high differential signal	VCCQ

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 3 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
UDC-	1	USB client low differential signal	VCCQ
SCL	1	I2C Clock	VCCQ
SDA	1	I2C Bidirectional Data	VCCQ
nRESET	1	Hardware reset	VCCQ
nRESET_OUT	1	Reset output	VCCQ
BOOT_SEL[2:0]	3	ROM Width Select (16/32)	VCCQ
PWR_EN	1	power enable	VCCQ
nBATT_FAULT	1	Battery Fault	VCCQ
nVDD_FAULT	1	VDD Fault	VCCQ
nTRST	1	JTAG Reset	VCCQ
TDI	1	JTAG Data In	VCCQ
TDO	1	JTAG Data Out	VCCQ
TMS	1	JTAG Mode Select	VCCQ
TCK	1	JTAG Clock	VCCQ
TESTCLK	1	TEST Clock	VCCQ
TEST	1	TEST mode	VCCQ
GP0	1	Reserved for sleep wakeup	VCCQ
GP1	1	Active low GP_reset	VCCQ
GP2	1	General Purpose I/O pin	VCCQ
GP3	1	General Purpose I/O pin	VCCQ
GP4	1	General Purpose I/O pin	VCCQ
GP5	1	General Purpose I/O pin	VCCQ
GP6	1	MMC Clock	VCCQ
GP7	1	48 mhz clock output	VCCQ
GP8	1	MMC Chip Select 0	VCCQ
GP9	1	MMC Chip Select 1	VCCQ
GP10	1	real time clock (1Hz)	VCCQ
GP11	1	3.6 MHz oscillator out	VCCQ
GP12	1	32 KHz out	VCCQ
GP13	1	memory controller grant	VCCQ
GP14	1	Alternate Bus Master Request	VCCQ
GP16	1	PWM0 output	VCCQ
GP17	1	PWM1 output	VCCQ

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 4 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
GP23	1	SSP clock	VCCQ
GP24	1	SSP Frame	VCCQ
GP25	1	SSP transmit	VCCQ
GP26	1	SSP receive	VCCQ
GP27	1	SSP ext_clk	VCCQ
GP28	1	AC97 bit_clk	VCCQ
		I2S bit_clk	
		I2S bit_clk	
		AC97 bit_clk	
GP29	1	AC97 Sdata_in0	VCCQ
		I2S Sdata_in	
GP30	1	I2S Sdata_out	VCCQ
		AC97 Sdata_out	
GP31	1	I2S sync	VCCQ
		AC97 sync	
GP32	1	I2S sysclk	VCCQ
		AC97 Sdata_in1	
GP34	1	FFUART receive	VCCQ
		MMC Chip Select 0	
GP35	1	FFUART Clear to send	VCCQ
GP36	1	FFUART Data carrier detect	VCCQ
GP37	1	FFUART data set ready	VCCQ
GP38	1	FFUART Ring Indicator	VCCQ
GP39	1	MMC Chip Select 1	VCCQ
		FFUART transmit data	
GP40	1	FFUART data terminal Ready	VCCQ
GP41	1	FFUART request to send	VCCQ
GP42	1	BTUART receive data	VCCQ
GP43	1	BTUART transmit data	VCCQ
GP44	1	BTUART clear to send	VCCQ
GP45	1	BTUART request to send	VCCQ
GP46	1	ICP receive data	VCCQ
		STD_UART receive data	

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 5 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
GP47	1	STD_UART transmit data	VCCQ
		ICP transmit data	
GP58	1	LCD data pin 0	VCCQ
GP59	1	LCD data pin 1	VCCQ
GP60	1	LCD data pin 2	VCCQ
GP61	1	LCD data pin 3	VCCQ
GP62	1	LCD data pin 4	VCCQ
GP63	1	LCD data pin 5	VCCQ
GP64	1	LCD data pin 6	VCCQ
GP65	1	LCD data pin 7	VCCQ
GP66	1	LCD data pin 8	VCCQ
		Alternate Bus Master Request	
GP67	1	LCD data pin 9	VCCQ
		MMC Chip Select 0	
GP68	1	MMC Chip Select 1	VCCQ
		LCD data pin 10	
GP69	1	MMC_CLK	VCCQ
		LCD data pin 11	
GP70	1	Real Time clock (1 Hz)	VCCQ
		LCD data pin 12	
GP71	1	3.6 MHz Oscillator clock	VCCQ
		LCD data pin 13	
GP72	1	32 KHz clock	VCCQ
		LCD data pin 14	
GP73	1	LCD data pin 15	VCCQ
		memory controller grant	
GP74	1	LCD Frame clock	VCCQ
GP75	1	LCD line clock	VCCQ
GP76	1	LCD Pixel clock	VCCQ
GP77	1	LCD AC Bias	VCCQ
GP81	1	NSSP serial clock	VCCQ
GP82	1	NSSP Frame	
GP83	1	NSSP Transmit/Receive	

Table 8-5. Intel® PXA26x Processor Family VCCN vs. VCCQ (Sheet 6 of 6)

Pin	Pin Count	Signal Description and Comments	Power Supply
GP84	1	NSSP Transmit/Receive	
GP85	1	General Purpose I/O pin	VCCQ
PXTAL	1	3.6 Mhz Crystal input	0.8 * VCC
PEXTAL	1	3.6 Mhz Crystal output	0.8 * VCC
TXTAL	1	32 Khz Crystal input	0.8 * VCC
TEXTAL	1	32 Khz Crystal output	0.8 * VCC

8.4.2 Power On Timing

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. This sequence is shown in Figure 8-1 and detailed in Table 8-6.

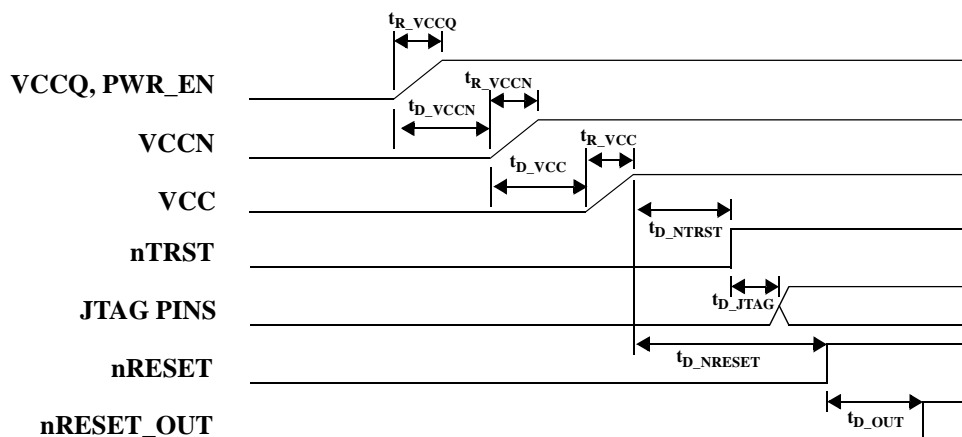
It is important that the processor power supplies be powered-up in a certain order to avoid high current situations. The required order is:

1. VCCQ
2. VCCN
3. VCC and PLL_VCC

VCCN may be powered at the same time as VCCQ, however do not apply power to VCCN before powering VCCQ.

Note: If hardware reset is entered during sleep mode, the proper power-supply stabilization times and nRESET timing requirements indicated in Table 8-6 must be observed.

Figure 8-1. Power-On Reset Timing



Note: 1) nBATT_FAULT and nVDD_FAULT must be high before nRESET_OUT is deasserted or the processor enters sleep mode.

Note: 2) The inclusion of PWR_EN is for informational purposes only to show its relationship to VCCQ. The use of PWR_EN to bring up VCCN or VCC at power-on reset is optional depending on the system's power management requirements. VCCN and VCC are not dependant on the PWR_EN signal being asserted.

Table 8-6. Power-On Timing Specifications

Symbol	Description	Min	Typical	Max
tR_VCCQ	VCCQ Rise / Stabilization time	0.01	—	100
tR_VCCN	VCCN Rise / Stabilization time	0.01	—	100
tR_VCC	VCC, PLL_VCC Rise / Stabilization time	0.01	—	10
tD_VCCN	Delay between VCCQ applied and VCCN applied	0	—	—
tD_VCC	Delay from VCCN applied and VCC, PLL_VCC applied	0	—	—
tD_NTRST	Delay between VCC, PLL_VCC stable and nTRST deasserted	50	—	—
tD_JTAG	Delay between nTRST deasserted and JTAG pins active, with nRESET asserted	0.03	—	—
tD_NRESET	Delay between VCC, PLL_VCC stable and nRESET deasserted	50	—	—
tD_OUT	Delay between nRESET deasserted and nRESET_OUT deasserted	18.1	—	18.2
tR_VCCQ	VCCQ Rise / Stabilization time	0.01	—	100

8.4.3 Hardware Reset Timing

The timing sequences shown in Figure 8-2 “Hardware Reset Timing” assumes the power supplies are stable at the assertion of nRESET. If the power supplies are unstable, follow the timings indicated in Section 8.4.2, “Power On Timing” on page 9.

Figure 8-2. Hardware Reset Timing

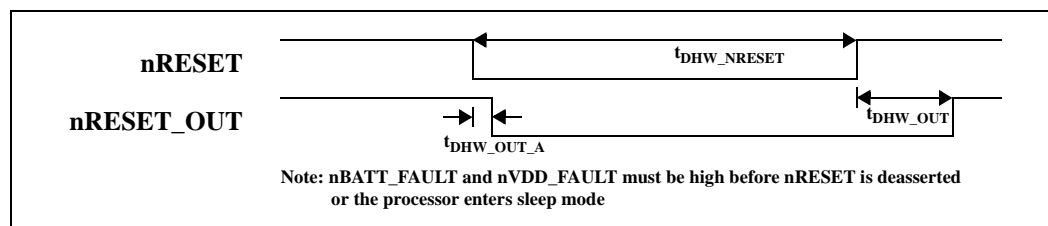


Table 8-7. Hardware Reset Timing Specifications

Symbol	Description	Min	Typical	Max
t _{DHW_NRESET}	Minimum assertion time of nRESET	0.001 ms	—	—
t _{DHW_OUT_A}	Delay between nRESET asserted and nRESET_OUT asserted	0 ms	—	0.001 ms
t _{DHW_OUT}	Delay between nRESET deasserted and nRESET_OUT deasserted	18.1 ms	—	18.2 ms
t _{DHW_NCS0}	Delay between nReset_Out and nCS0	400 ns	—	420 ns

8.4.4 Watchdog Reset Timing

Watchdog reset is an internally generated reset and therefore has no external pin dependencies. The nRESET_OUT pin is the only indicator of watchdog reset, and it stays asserted for t_{DHW_OUT} . Refer to Figure 8-2 for more information.

8.4.5 GPIO Reset Timing

GPIO reset is generated externally. The pin used as the GPIO reset is reconfigured as a standard GPIO after the reset propagates internally. Because the clock module is not reset by GPIO reset, timing varies based on the frequency of the selected clock. Timing also varies in the frequency change sequence (see Section 8.3.1). Figure 8-3 shows the possible GPIO reset timing.

Figure 8-3. GPIO Reset Timing

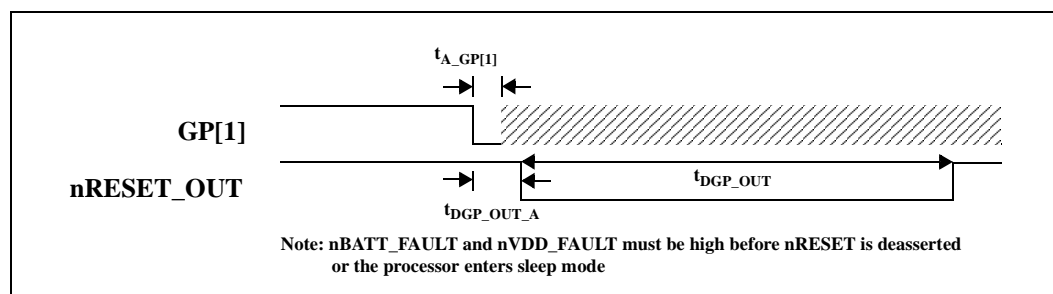


Table 8-8. GPIO Reset Timing Specifications

Symbol	Description	Min	Typical	Max
$t_{A_GP[1]}$	Minimum assert time of GP[1] ¹ in 3.6864 MHz input clock cycles	4 cycles	—	—
$t_{DGP_OUT_A}$	Delay between GP[1] Asserted and nRESET_OUT asserted in 3.6864 MHz input clock cycles	3 cycles	—	8 cycles
t_{DGP_OUT}	Delay between nRESET_OUT asserted and nRESET_OUT deasserted, run or turbo mode ²	1.28 μ s	—	6.5 μ s
$t_{DGP_OUT_F}$	Delay between nRESET_OUT asserted and nRESET_OUT deasserted, during the frequency change sequence ³	1.28 μ s	—	360 μ s
t_{DGP_NCS0}	Delay between nReset_Out and nCS0	150.69 ns	—	390 ns

NOTES:

- GP[1] is not recognized as a reset source again until configured to do so in software. Software should check the state of GP[1] before configuring it as a reset to ensure no spurious reset is generated.
- Time is 512*N processor clock cycles plus as many as 4 cycles of the 3.6864 MHz input clock.
- Time during the frequency change sequence depends on the state of the PLL lock detector at the assertion of GPIO Reset. The lock detector has a maximum time of 350 μ s plus synchronization.

8.4.6 Sleep Mode Timing

Sleep mode is internally asserted, and asserts the nRESET_OUT and PWR_EN signals. The sequence indicated in Figure 8-4 and detailed in Table 8-9 are the required timing parameters for sleep mode.

Figure 8-4. Sleep Mode Timing

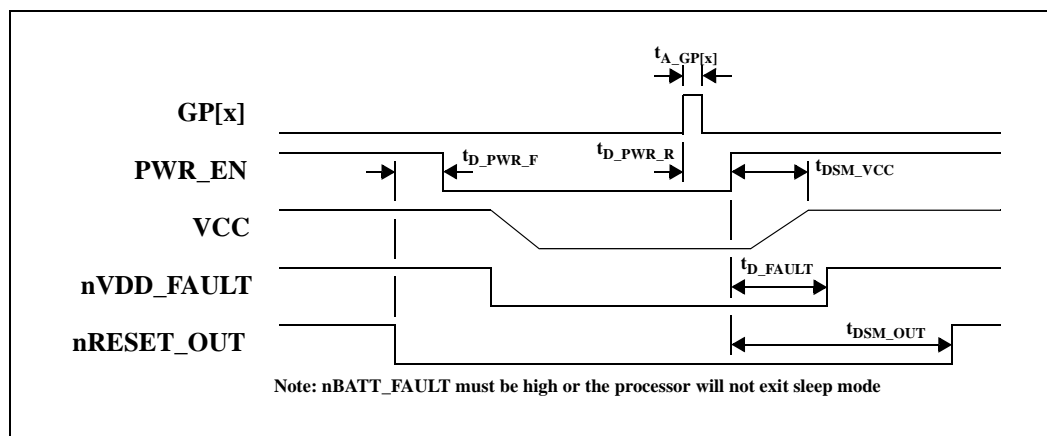


Table 8-9. Sleep Mode Timing Specifications

Symbol	Description	Min	Typical	Max
$t_{A_GP[x]}$	Assert Time of GPIO Wake up Source (x=[15:0])	91.6 μ s	—	—
$t_{D_PWR_F}$	Delay from nRESET_OUT asserted to PWR_EN deasserted	61 μ s	—	91.6 μ s
$t_{D_PWR_R}$	Delay between GP[x] asserted to PWR_EN asserted	30.5 μ s	—	122.1 μ s
t_{DSM_VCC}	Delay between PWR_EN asserted and VCC stable	—	—	10 ms
t_{DSM_NCS0}	Delay between nReset_Out and nCS0	180.84 ns	—	332 ns
t_{D_FAULT}	Delay between PWR_EN asserted and nVDD_FAULT deasserted	—	—	10 ms
t_{DSM_OUT}	Delay between PWR_EN asserted and nRESET_OUT deasserted, OPDE Set	28.0 ms	—	28.5 ms
$t_{DSM_OUT_O}$	Delay between PWR_EN asserted and nRESET_OUT deasserted, OPDE Clear	10.35 ms	—	10.5 ms

8.5 Memory Bus and PCMCIA AC Specifications

This section gives the timing information for these types of memory:

- SRAM / ROM / flash / Synchronous fast flash asynchronous writes (Table 8-10)
- Variable Latency I/O (Table 8-11)
- Card Interface (PCMCIA or Compact Flash) (Table 8-12)
- Synchronous Memories (Table 8-13)

Table 8-10. SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications

Symbol	Description	MEMCLK Frequency (MHz)					Notes
		99.5	118.0	132.7	147.5	165.9	
SRAM / ROM / Flash / Synchronous Fast Flash (WRITES) (Asynchronous)							
tromAS	MA(25:0) setup to nCS, nOE, nSDCAS (as nADV) asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromAH	MA(25:0) hold after nCS, nOE, nSDCAS (as nADV) deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromASW	MA(25:0) setup to nWE asserted	30 ns	25.5 ns	22.5 ns	20.4 ns	18 ns	2
tromAHW	MA(25:0) hold after nWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromCES	nCS setup to nWE asserted	20 ns	17 ns	15 ns	13.6 ns	12 ns	3
tromCEH	nCS hold after nWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromDS	MD(31:0), DQM(3:0) write data setup to nWE asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromDSWH	MD(31:0), DQM(3:0) write data setup to nWE deasserted	20 ns	17 ns	15 ns	13.6 ns	12 ns	3
tromDH	MD(31:0), DQM(3:0) write data hold after nWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tromNWE	nWE high time between beats of write data	20 ns	17 ns	15 ns	13.6 ns	12 ns	3

NOTES:

1. This number represents 1 MEMCLK period
2. This number represents 3 MEMCLK periods
3. This number represents 2 MEMCLK periods

Table 8-11. Variable Latency I/O Interface AC Specifications (Sheet 1 of 2)

Symbol	Description	MEMCLK Frequency (MHz)					Notes
		99.5	118.0	132.7	147.5	165.9	
Variable Latency IO Interface (VLIO) (Asynchronous)							
tvlioAS	MA(25:0) setup to nCS asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioASRW	MA(25:0) setup to nOE or nPWE asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioAH	MA(25:0) hold after nOE or nPWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioCES	nCS setup to nOE or nPWE asserted	20 ns	17 ns	15 ns	13.6 ns	12 ns	2
tvlioCEH	nCS hold after nOE or nPWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioDSW	MD(31:0), DQM(3:0) write data setup to nPWE asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioDSWH	MD(31:0), DQM(3:0) write data setup to nPWE deasserted	20 ns	17 ns	15 ns	13.6 ns	12 ns	2
tvlioDHW	MD(31:0), DQM(3:0) hold after nPWE deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tvlioDHR	MD(31:0) read data hold after nOE deasserted	0 ns	0 ns	0 ns	0 ns	0 ns	—

Table 8-11. Variable Latency I/O Interface AC Specifications (Sheet 2 of 2)

Symbol	Description	MEMCLK Frequency (MHz)					Notes
		99.5	118.0	132.7	147.5	165.9	
tvlioRDYH	RDY hold after nOE, nPWE deasserted	0 ns	0 ns	0 ns	0 ns	0 ns	—
tvlioNPWE	nPWE, nOE high time between beats of write or read data	20 ns	17 ns	15 ns	13.6 ns	12 ns	2

NOTES:

1. This number represents 1 MEMCLK period
2. This number represents 2 MEMCLK periods

Table 8-12. Card Interface (PCMCIA or Compact Flash) AC Specifications

Symbol	Description	MEMCLK Frequency (MHz)					Notes
		99.5	118.0	132.7	147.5	165.9	
Card Interface (PCMCIA or Compact Flash) (Asynchronous)							
tcardAS	MA(25:0), nPREG, PSKTSEL, nPCE setup to nPWE, nPOE, nPIOW, or nPIOR asserted	20 ns	17 ns	15 ns	13.6 ns	12 ns	1
tcardAH	MA(25:0), nPREG, PSKTSEL, nPCE hold after nPWE, nPOE, nPIOW, or nPIOR deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tcardDS	MD(31:0) setup to nPWE, nPOE, nPIOW, or nPIOR asserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tcardDH	MD(31:0) hold after nPWE, nPOE, nPIOW, or nPIOR deasserted	10 ns	8.5 ns	7.5 ns	6.8 ns	6 ns	1
tcardCMD	nPWE, nPOE, nPIOW, or nPIOR command assertion	30 ns	25.5 ns	22.5 ns	20.4 ns	18 ns	1

NOTE:

1. These numbers are minimums. They can be much longer based on the programmable Card Interface timing registers.

Table 8-13. Synchronous Memory Interface AC Specifications (Sheet 1 of 2)

Symbol	Description	MIN	MAX	Notes ¹
SDRAM / SMROM				
tsynCLK	SDCLK period	10 ns	20 ns	2
tsynCMD	nSDCAS, nSDRAS, nWE, nSDCS assert time	1 sdclk	—	—
tsynRCD	nSDRAS to nSDCAS assert time	1 sdclk	—	—
tsynCAS	nSDCAS to nSDCAS assert time	2 sdclk	—	—
tsynSDOS	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output setup time to SDCLK(2:0) rise	5 ns	—	3
tsynSDOH	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output hold time from SDCLK(2:0) rise	5 ns	—	3
tsynSDIS	MD(31:0) read data input setup time from SDCLK(2:0) rise	0.5 ns	—	—
tsynDIH	MD(31:0) read data input hold time from SDCLK(2:0) rise	1.5 ns	—	—
Fast Flash (Synchronous READS only)				
tffCLK	SDCLK period	15 ns	20 ns	4
tffAS	MA(25:0) setup to nSDCAS (as nADV) asserted	0.5 sdclk	—	—

Table 8-13. Synchronous Memory Interface AC Specifications (Sheet 2 of 2)

Symbol	Description	MIN	MAX	Notes ¹
tffCES	nCS setup to nSDCAS (as nADV) asserted	0.5 sdclk	—	—
tffADV	nSDCAS (as nADV) pulse width	1 sdclk	—	—
tffOS	nSDCAS (as nADV) deassertion to nOE assertion	3 sdclk	—	—
tffCEH	nOE deassertion to nCS deassertion	4 sdclk	—	—

NOTES:

1. These numbers are for a maximum 99.5 MHz MEMCLK and 99.5 MHz output SDCLK.
2. SDCLK for SDRAM and SMROM can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be 99.5 MHz at the fastest.
3. This number represents 1/2 SDCLK period.
4. SDCLK for fast flash can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be divide-by-2 of the 132.7 MHz MEMCLK at its fastest.

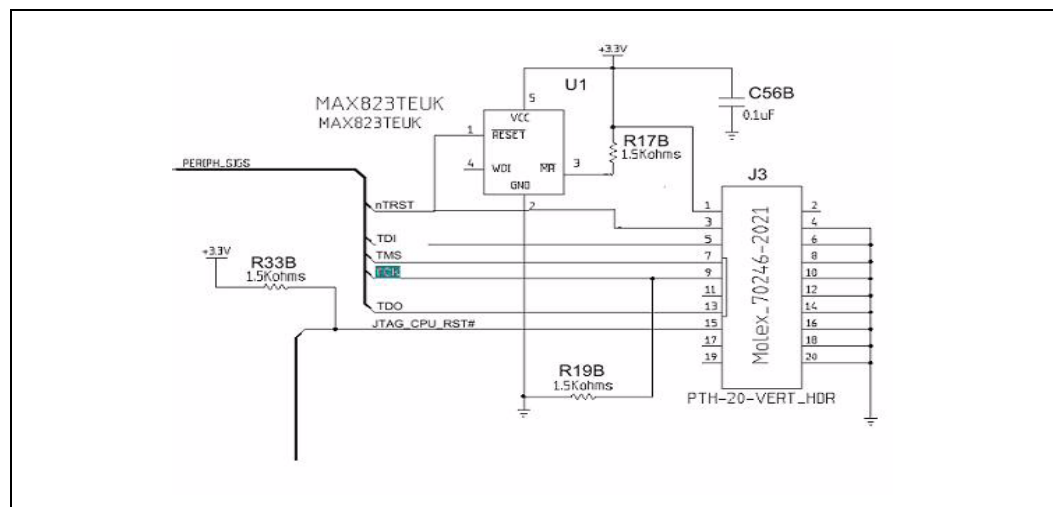
9.1 Description

The JTAG/Debug port is essentially several shift registers, with the destination controlled by the TMS pin and data I/O with TDI/TDO. nTRST provides initialization of the test logic. JTAG is testable via the IEEE 1149.1. Many use JTAG to control the address/data bus for flash programming. JTAG is also a hardware debug port.

9.2 Schematics

All JTAG pins, except for nTRST and TCK, are directly connected. TCK is not driven internally and so you must add an external pull-up or pull-down resistor. Intel recommends adding a 1.5 k pull-down resistor to TCK. nTRST must be asserted during power-on. Asserting nRESET or nTRST must not cause the other reset signal to assert. Also, use an external pull-up resistor on nTRST to prevent spurious resets of the JTAG port when disconnected. The circuit in Figure 9-1 drives nTRST. It uses a reset IC on nTRST to ensure that nTRST is reset at power-on. nRESET must be directly connected to the CPU nRESET. Do not connect pins 17 and 19 – they are special purpose functions and not used.

Figure 9-1. JTAG/Debug Port Wiring Diagram



If you are not utilizing either JTAG or the hardware debug functions, it is highly recommended that you design in a JTAG/debug port on your system. This greatly facilitates board debug, startup, and software development. During final production you do not have to populate the JTAG connector.

9.3 Layout

Use the JTAG/Debug the port layout recommendations given in ARM's application note, *Multi-ICE System Design Considerations, Application Note 72*. The recommended connector is a 2x10-way, 2.54 mm pitch pin header, shown in Figure 9-1.

If board space is critical, use a small form-factor receptacle with a smaller pitch. Then use a cable interface that has a wire “dongle” with a 2.54 mm pitch pin header on one end and the smaller pitch connector on the other.

Place the JTAG/Debug connector as close as possible to the processor to minimize signal degradation.



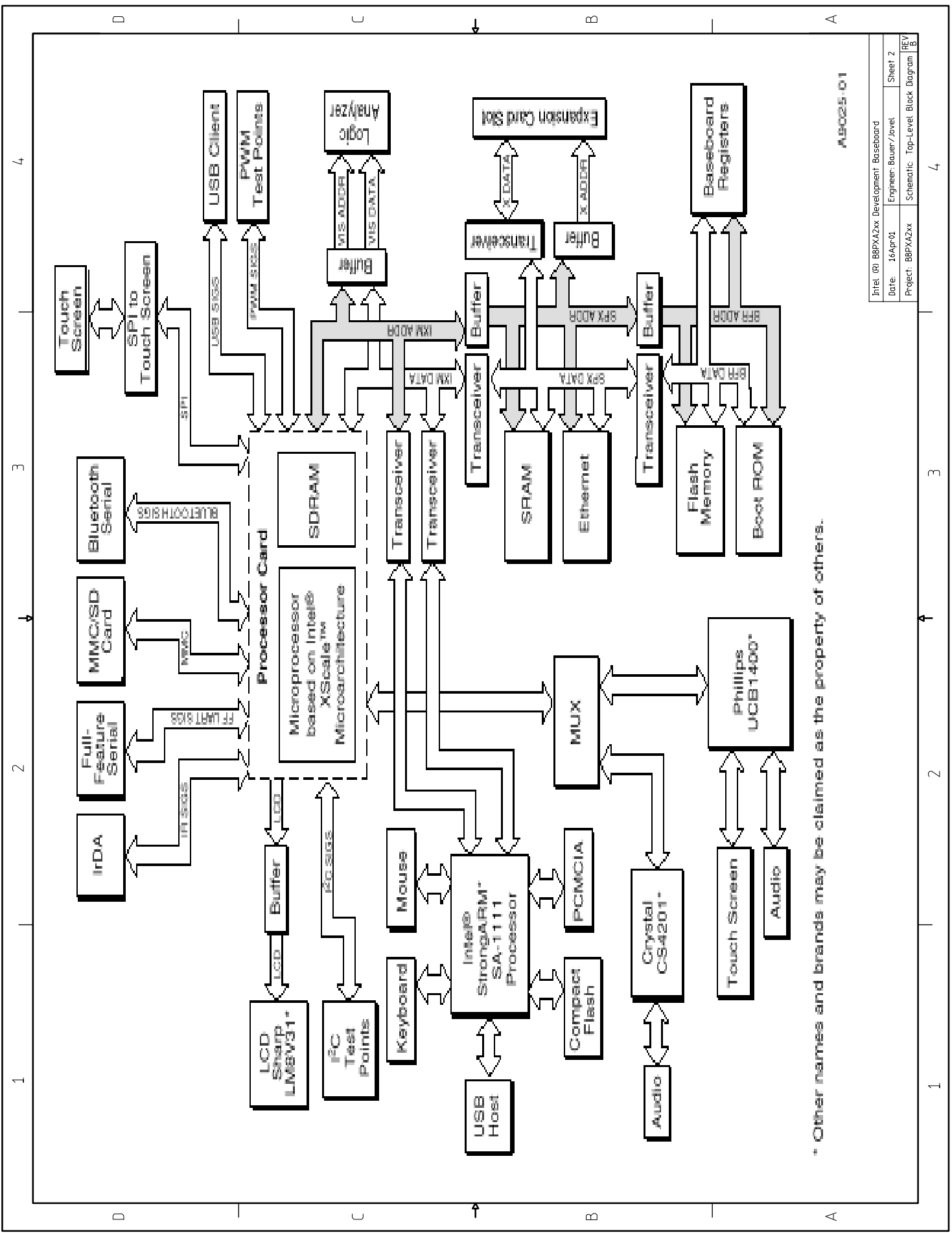
BBPXA2xx Development Baseboard Schematic Diagrams

A

Intel (R) BBPA2xx Development Baseboard

Table of Contents

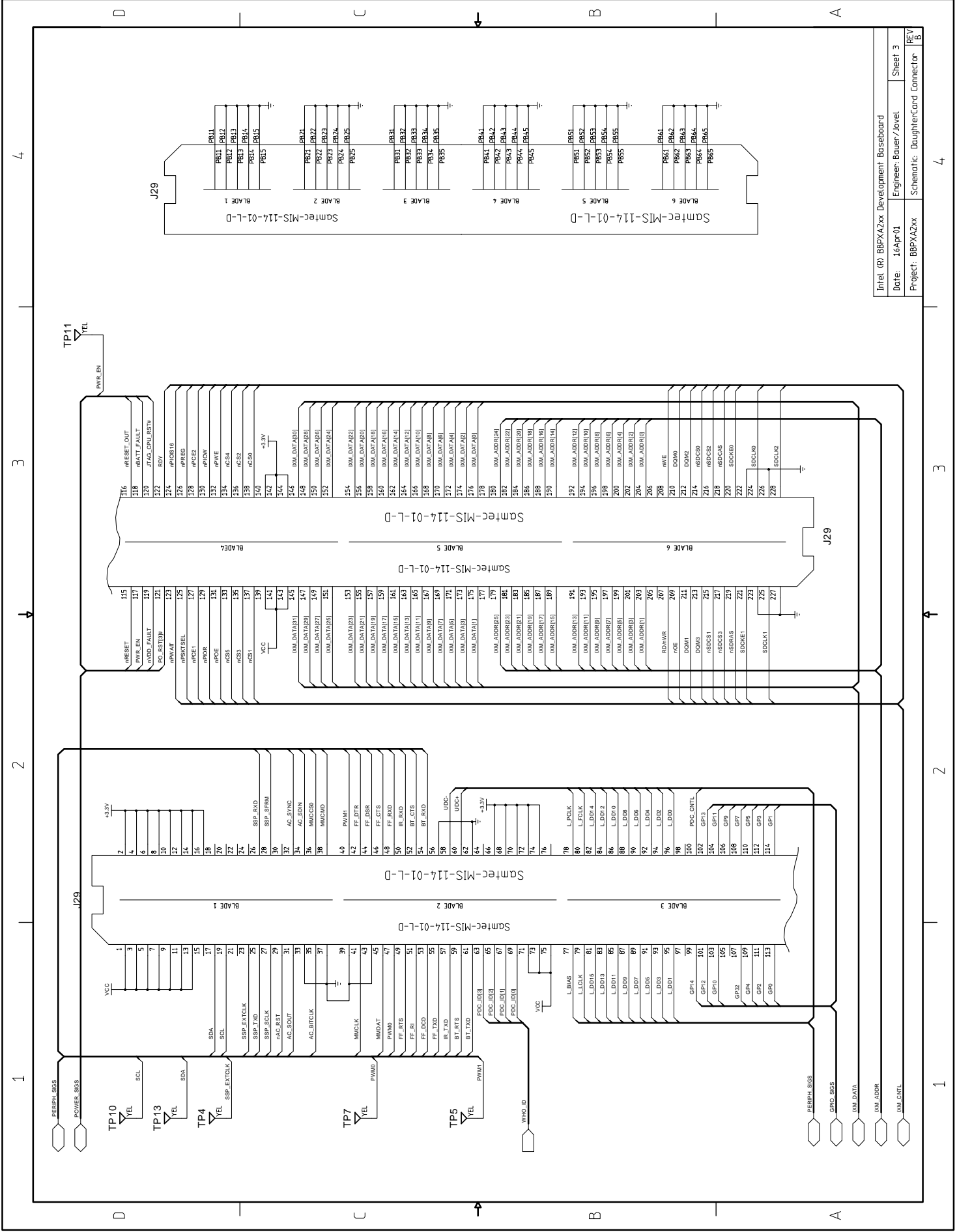
Page	Function	Page	Function	Page	Function
2	Top level block diagram	18	SWITCHES	34	LOGIC ANALYZER
3	DaughterCard Connector	19	SPII SPROM	35	RESET & FAULT SWITCHES
4	Data Buffers/Transceivers	20	SA-1111 INTERFACE	36	3.3V & 5V SUPPLY
5	Data Buffers/Transceivers	21	CF & PCMCIA I/O	37	POWER SUPPLY INPUT
6	Address BUFFERS/TRANSCIVERS	22	CF & PCMCIA PU	38	SPARES
7	SPX ADDRESS BUFFERS	23	SA-1111 USB KB/MS		
8	CONTROL BUFFERS/TRANSCIVERS	24	BUFFER CONTROL LOGIC		
9	X ADDRESS BUFFERS	25	LCD BUFFERS		
10	BFR ADDRESS BUFFERS	26	IrDA & FF SERIAL & USB		
11	SRAM	27	CS4201 CODEC		
12	FLASH	28	UCB1400 CODEC		
13	ROM	29	BB TOUCH SCREEN & GPIO HEADER		
14	REGISTER & CONTROL	30	CODEC MUX & SPII 2.5V		
15	HEX DISPLAY HIGH	31	SDCARD & BT SERIAL		
16	HEX DISPLAY LOW	32	10Mbps ETHERNET		
17	LEDs & HEX SWITCHES	33	XPANSION PORT		

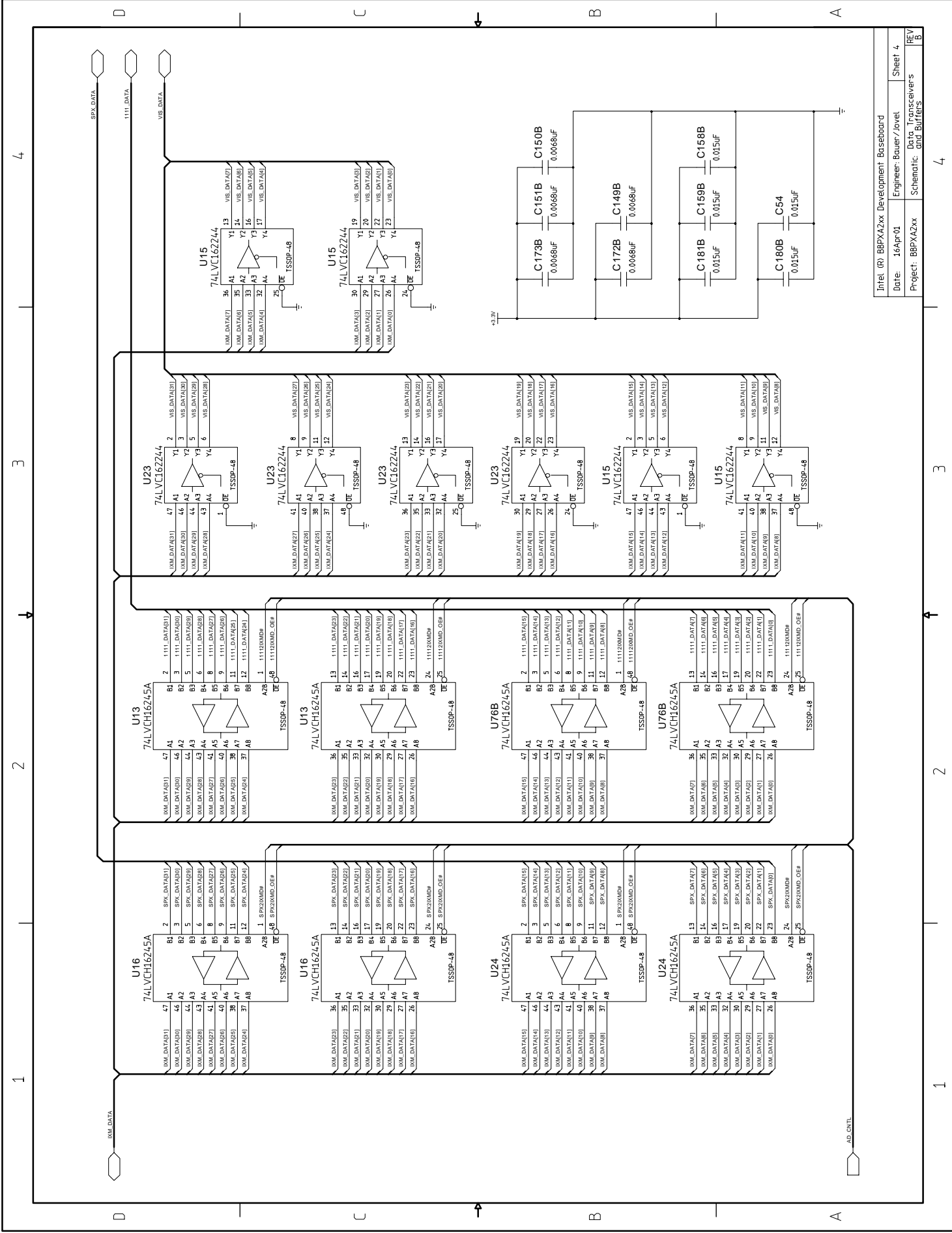


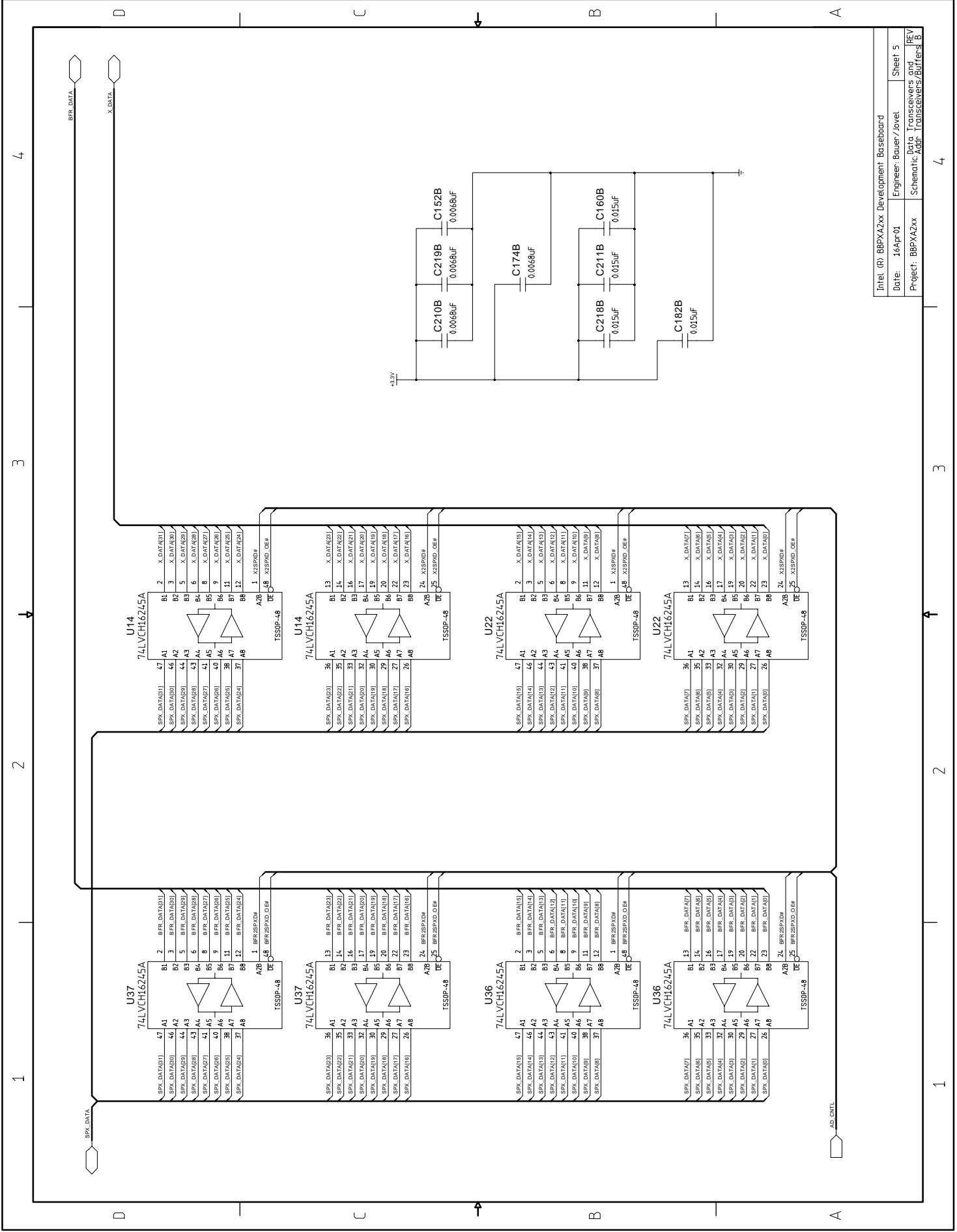
* Other names and brands may be claimed as the property of others.

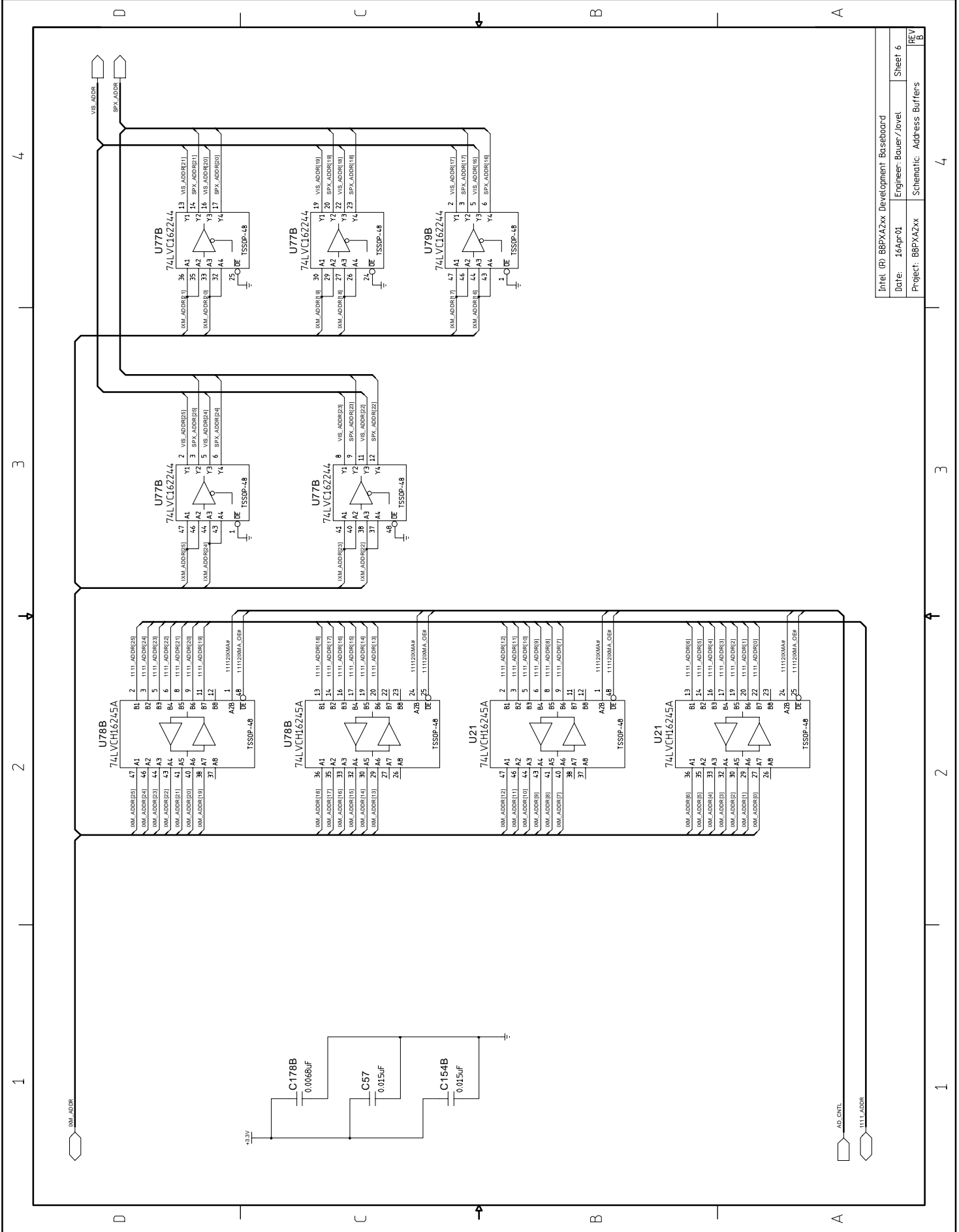
A9025-01

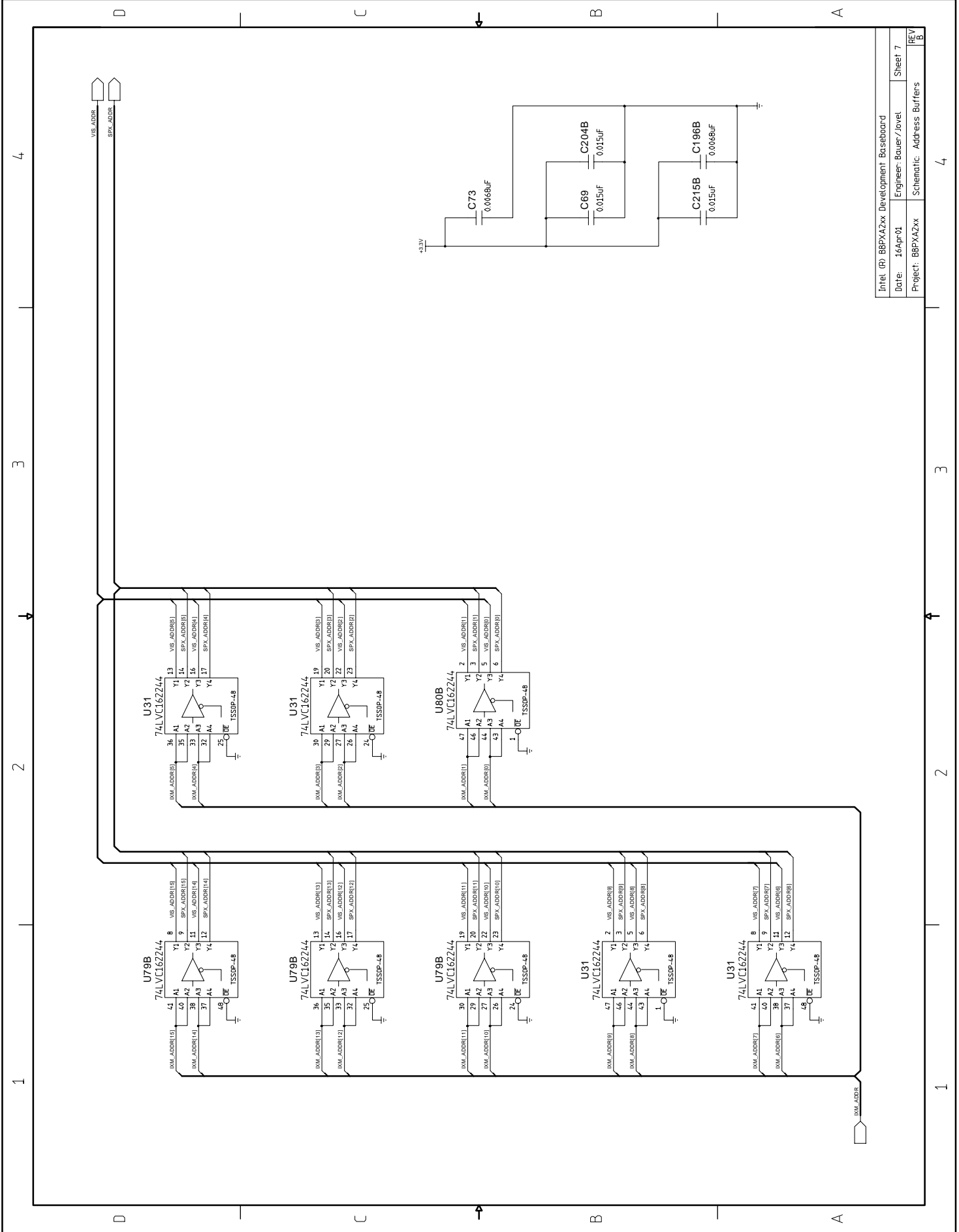
Intel (R) 88PXA2xx Development Baseboard			
Date:	16Apr01	Engineer:	Bauer/Jovel
Project:	88PXA2xx	Schematic:	Top-Level Block Diagram
		REV	18

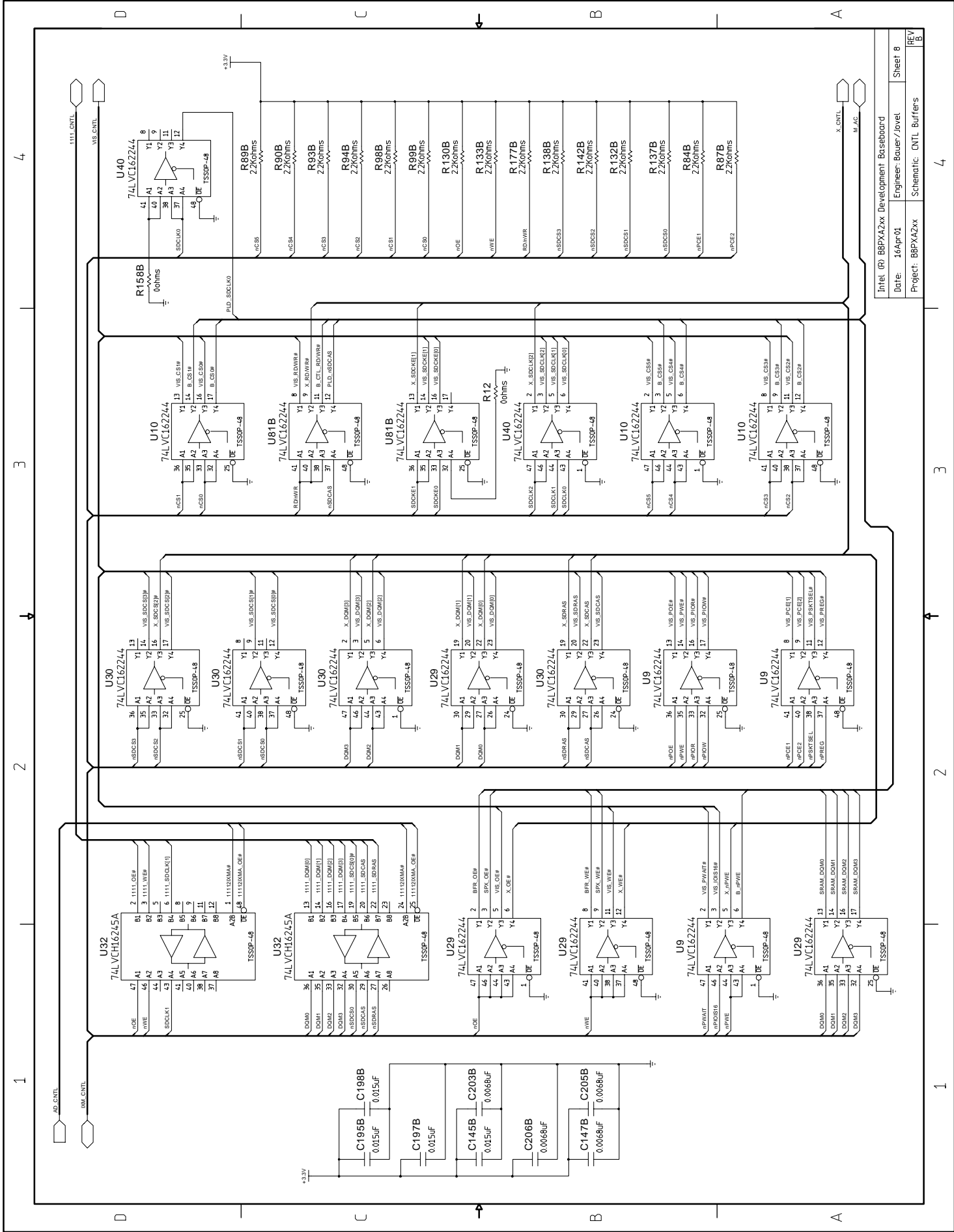


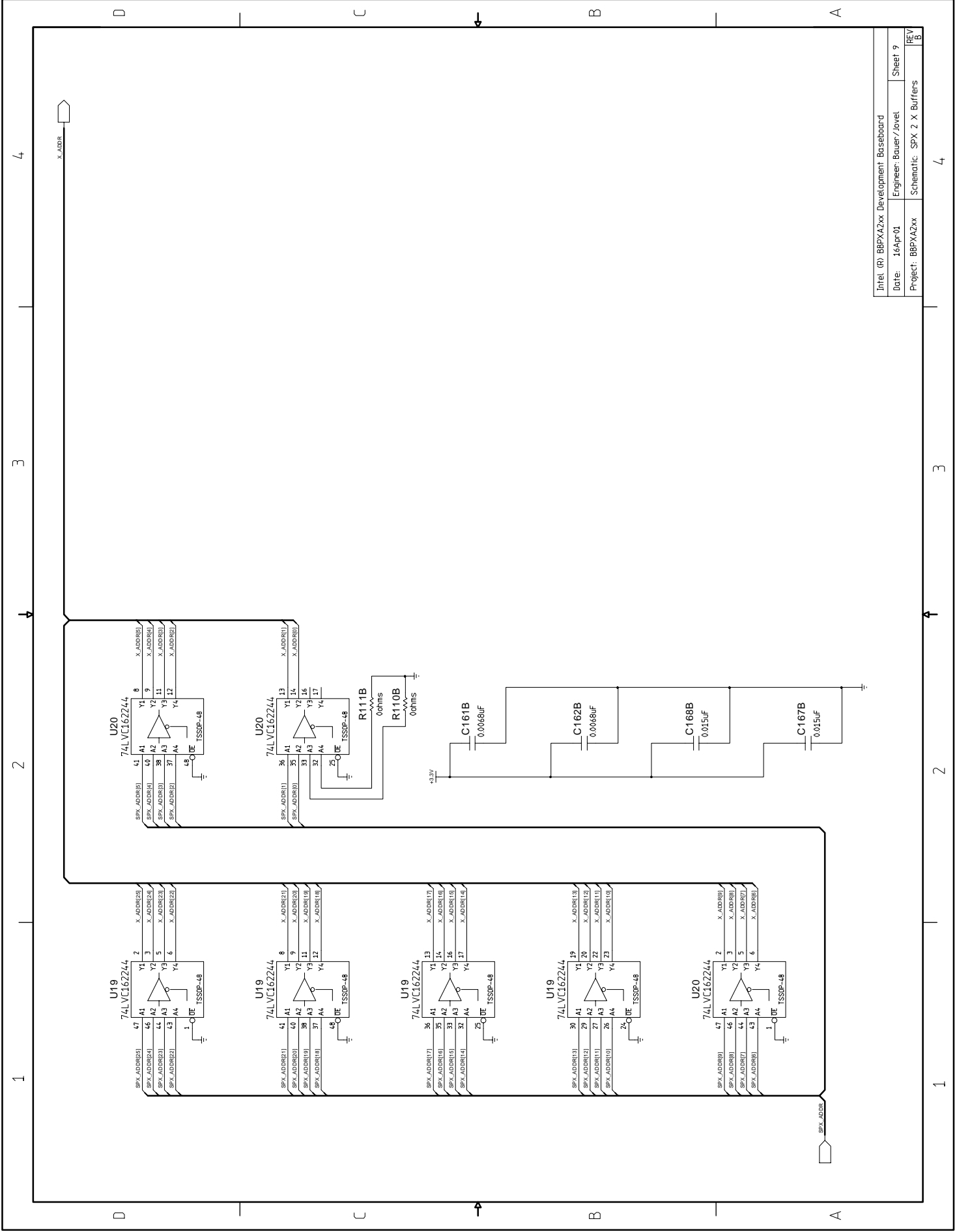




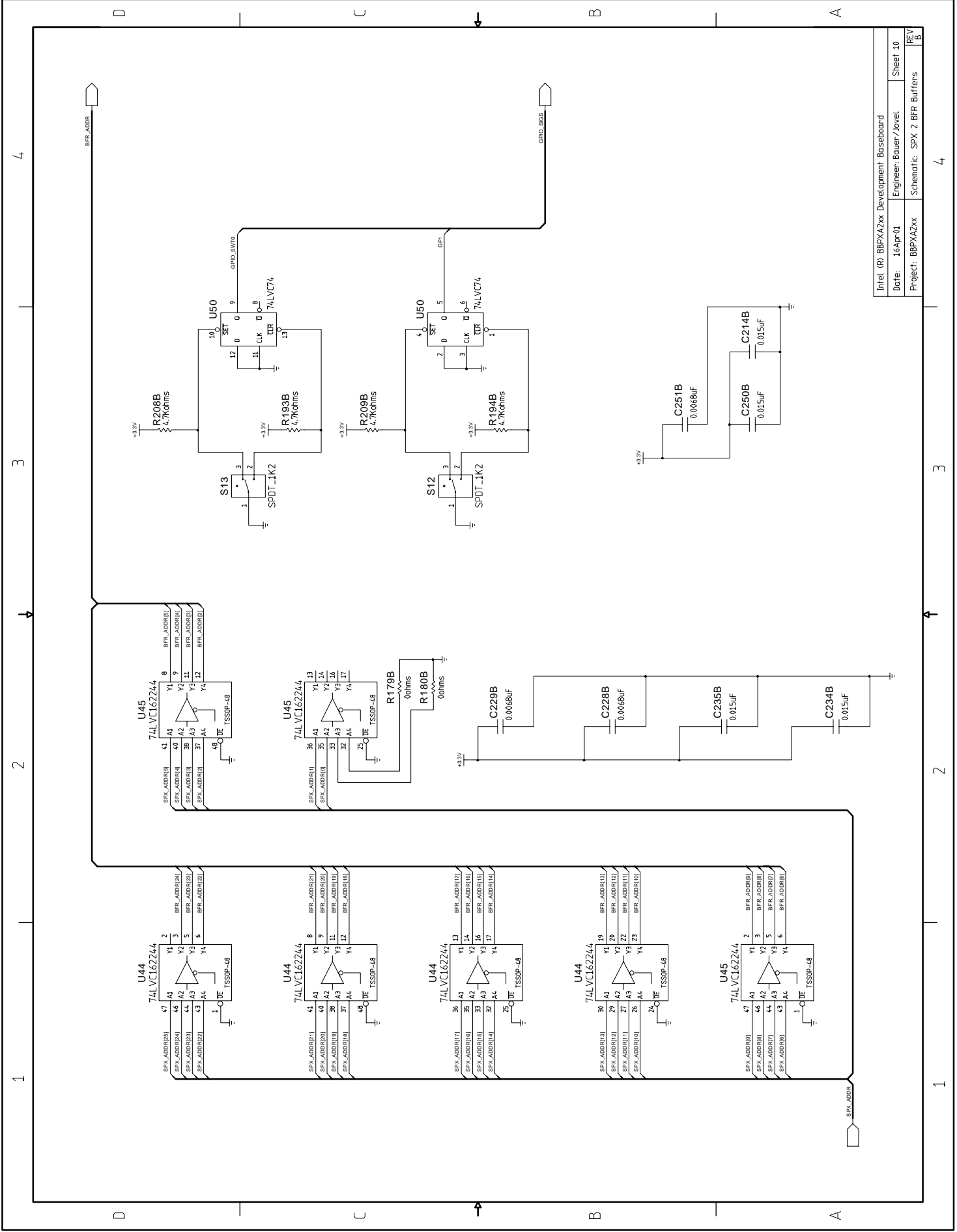




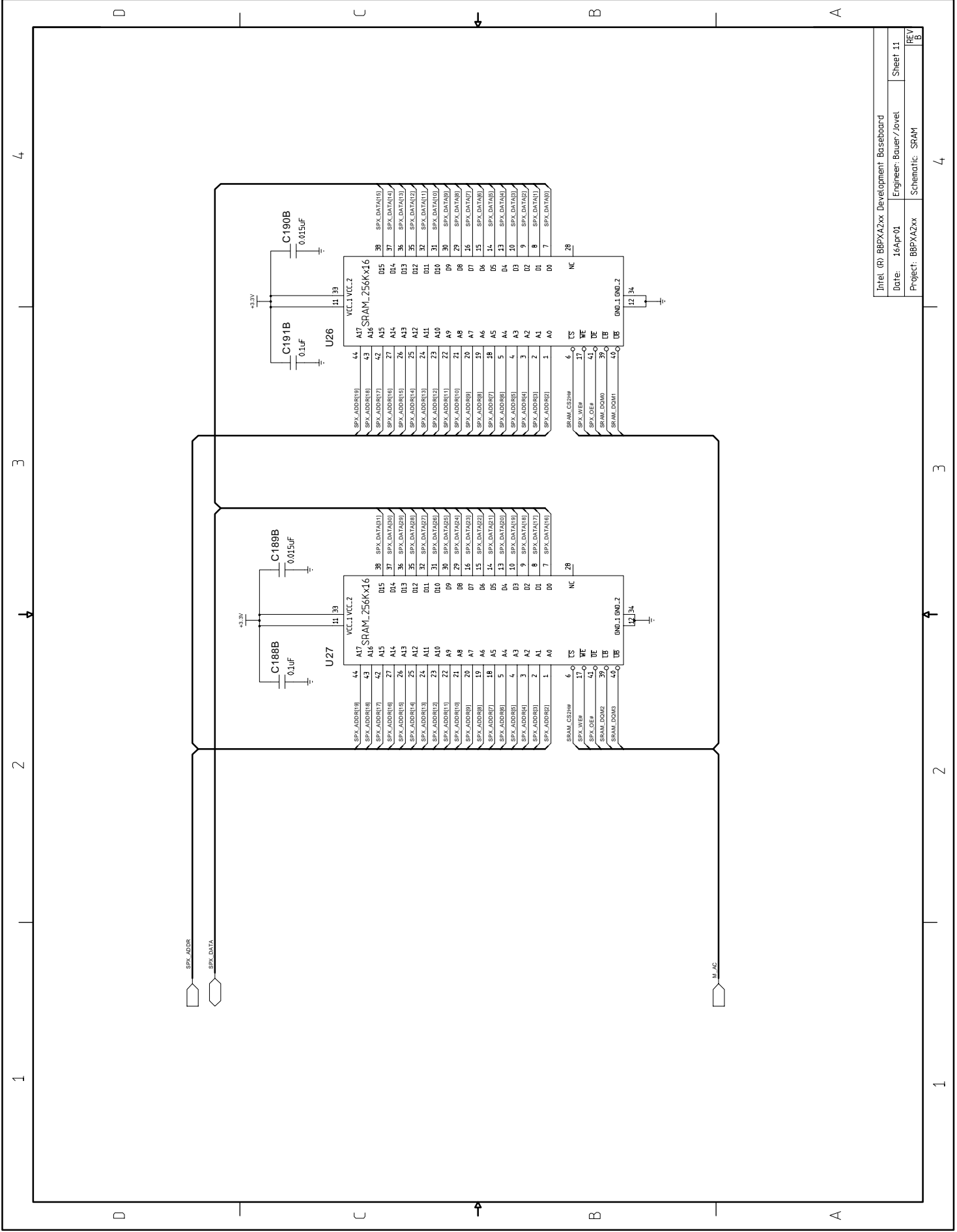




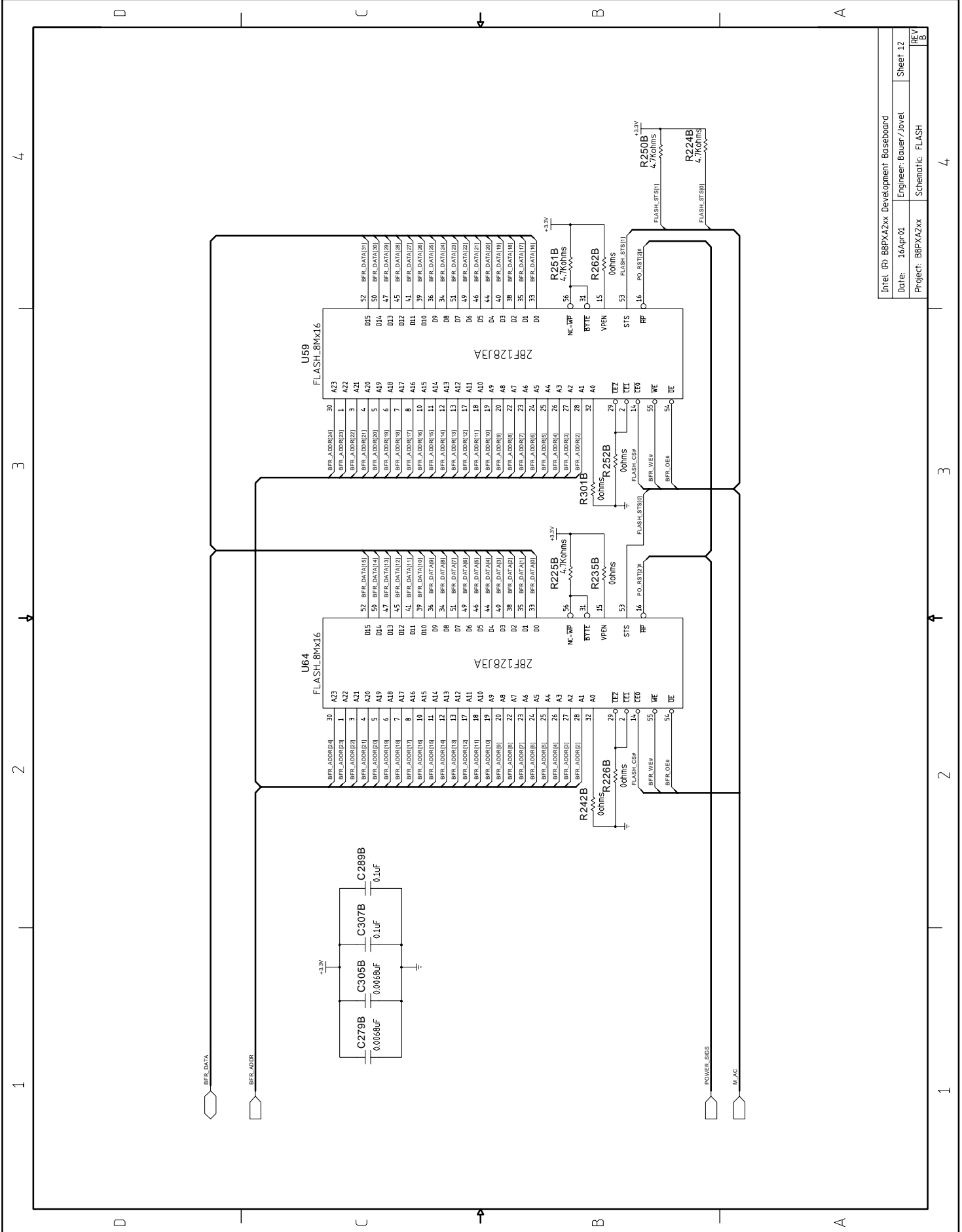
Intel (R) B8PXA2xx Development Baseboard		
Date: 16Apr01	Engineer: Bauer/Jovel	Sheet: 9
Project: B8PXA2xx	Schematic: SPX_2_X_Buffers	REV: B



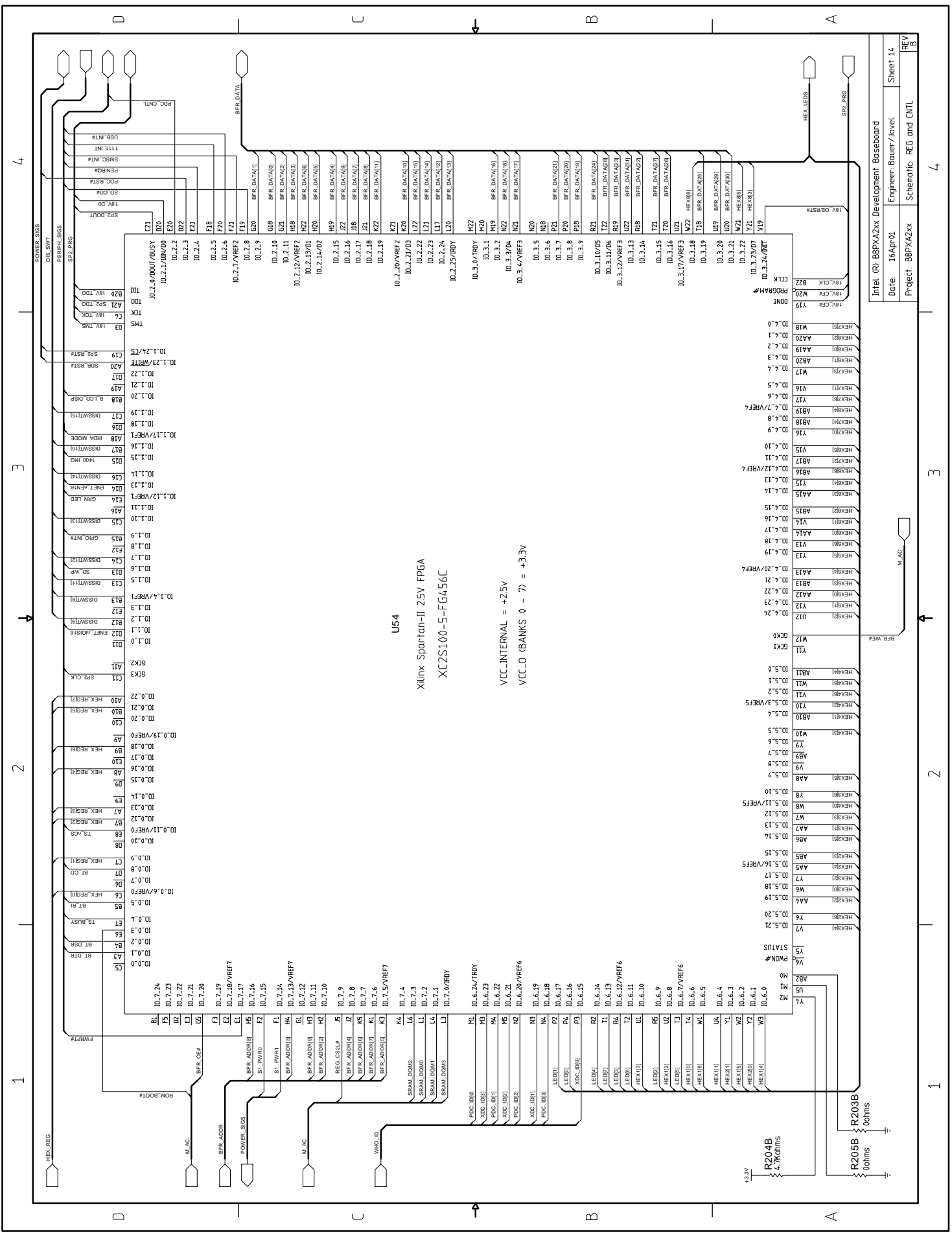
Intel (R) B8PXA2xx Development Baseboard		
Date:	16Apr01	Sheet 10
Project:	B8PXA2xx	Schematic: SPX 2 BFR Buffers
REV	B	

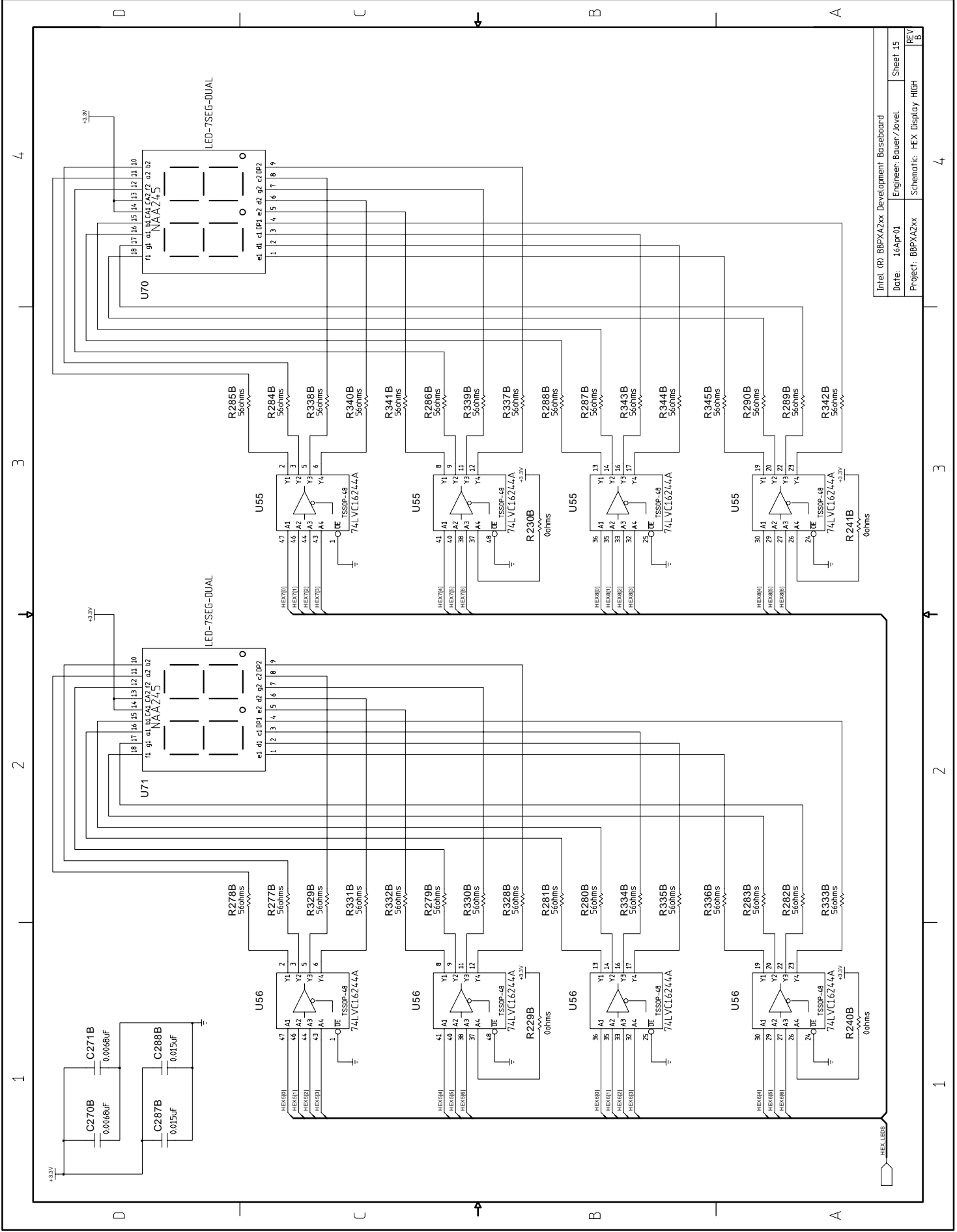


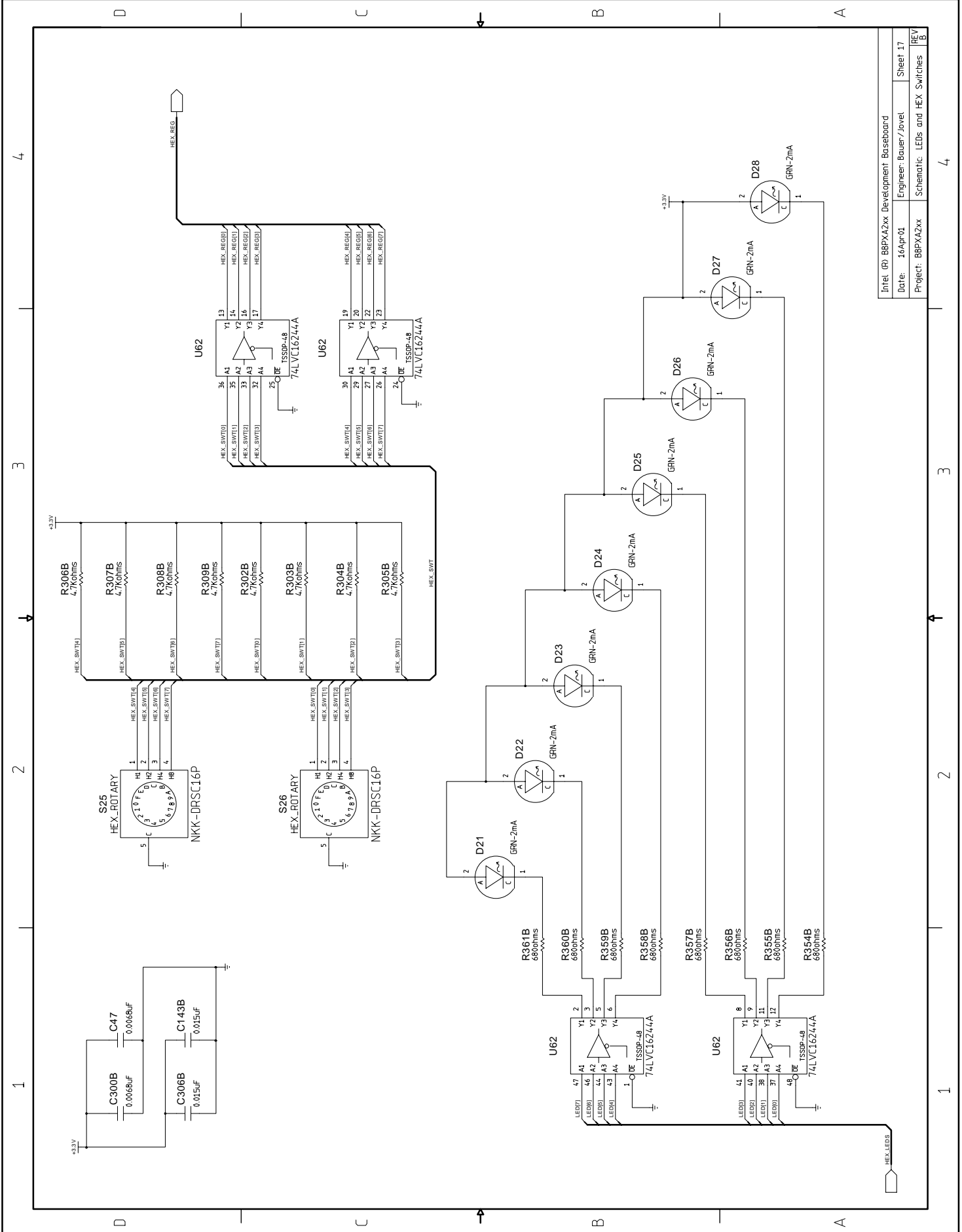
Intel (R) BBPXA2xx Development Baseboard		
Date: 16Apr01	Engineer: Bauer/Jovel	Sheet 11
Project: BBPXA2xx	Schematic: SRAM	REV B

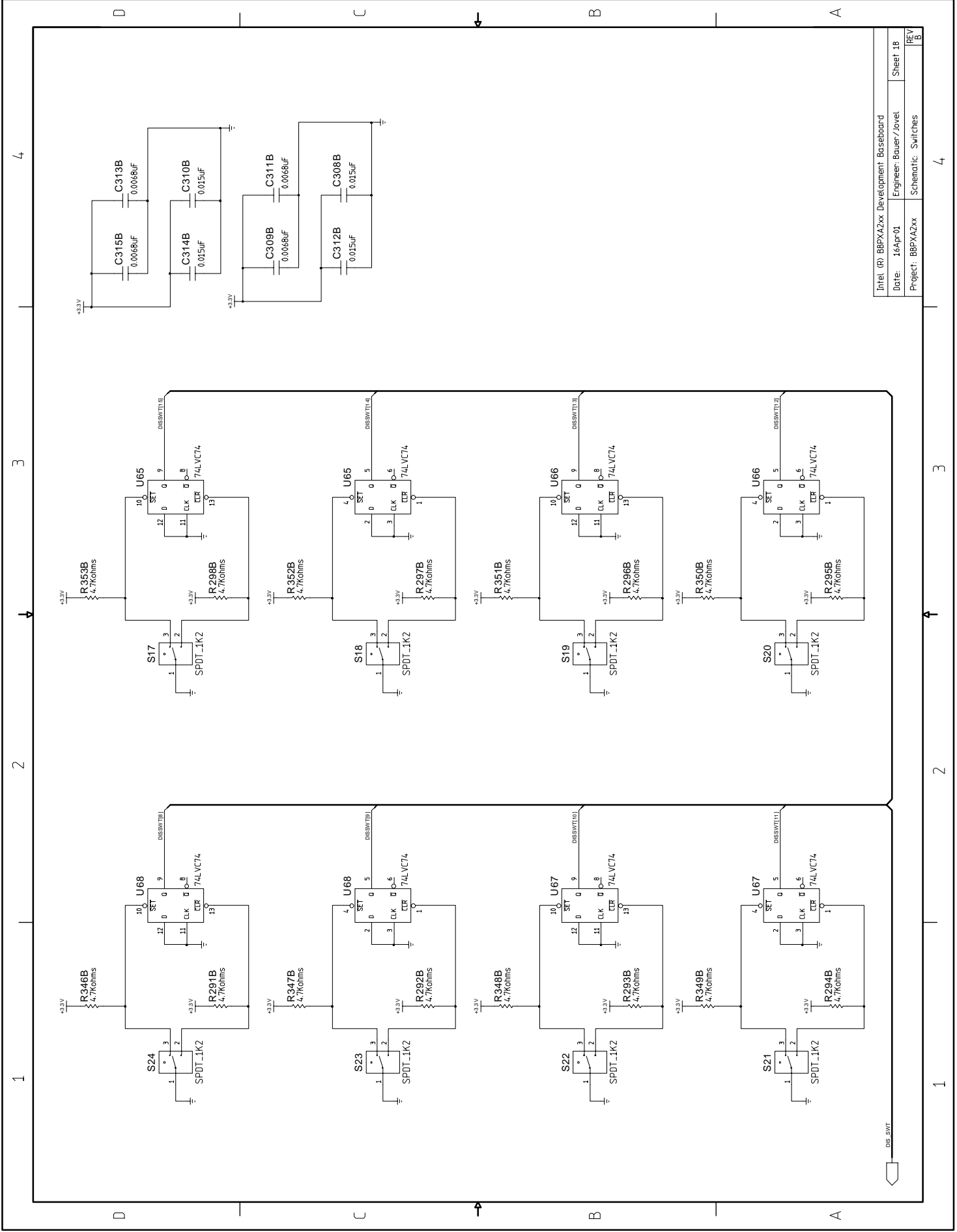


Intel (R) BBPX2xx Development Baseboard		
Date: 16Apr01	Engineer: Bauer/Jovel	Sheet 12
Project: BBPX2xx	Schematic: FLASH	REV B

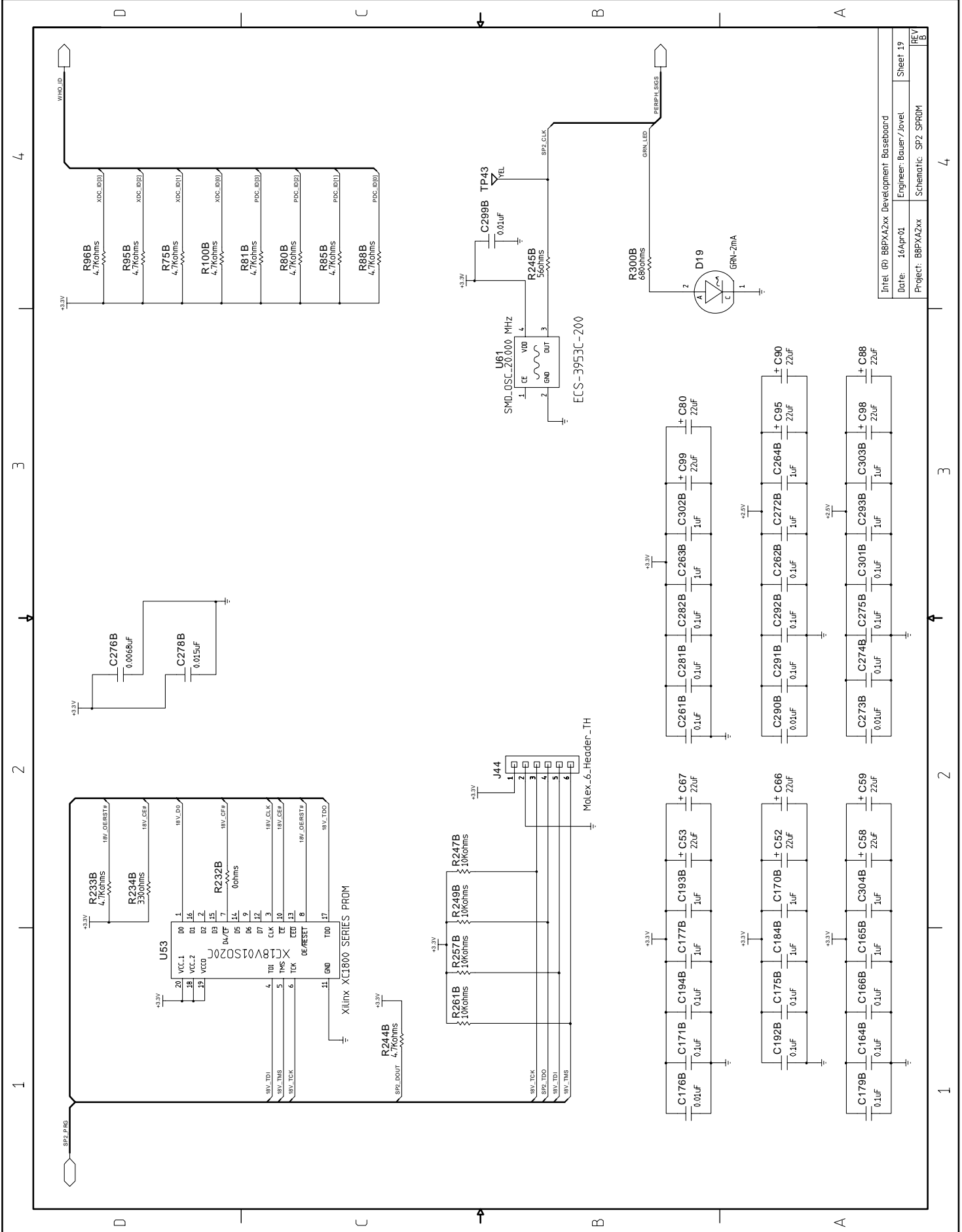




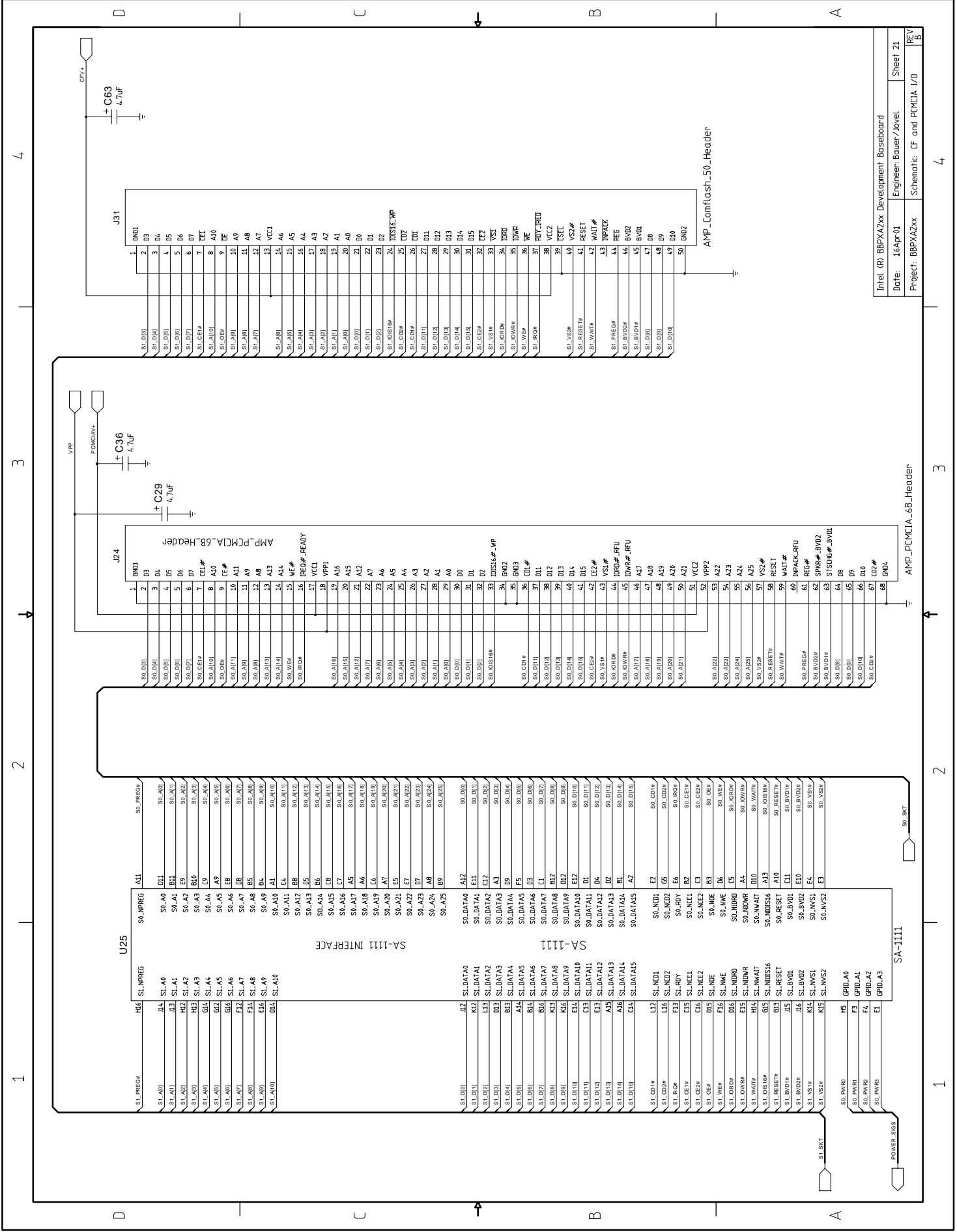


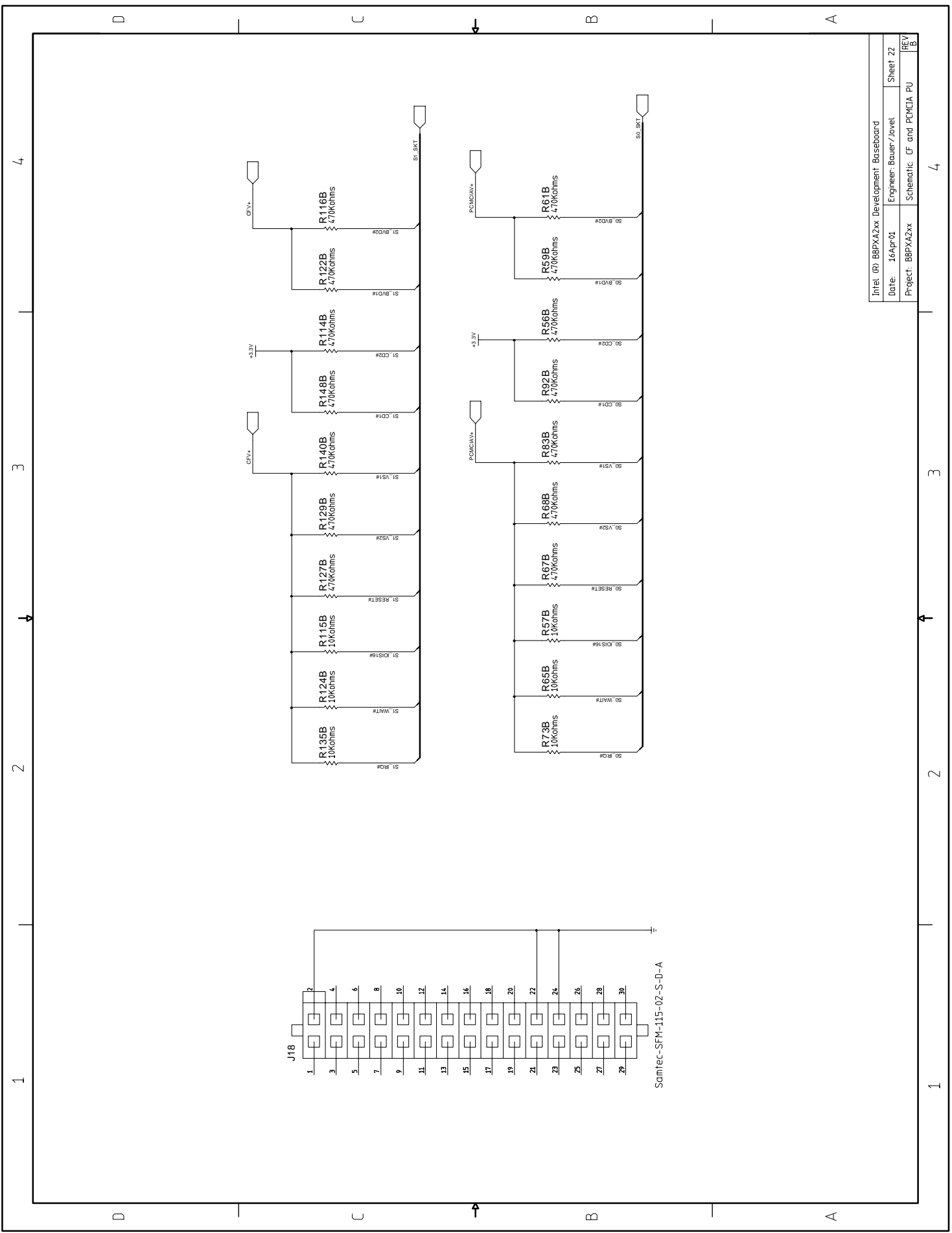


Intel (R) BBPXA2xx Development Baseboard		
Date:	16Apr01	Sheet 18
Project:	BBPXA2xx	Schematic: Switches
REV		B

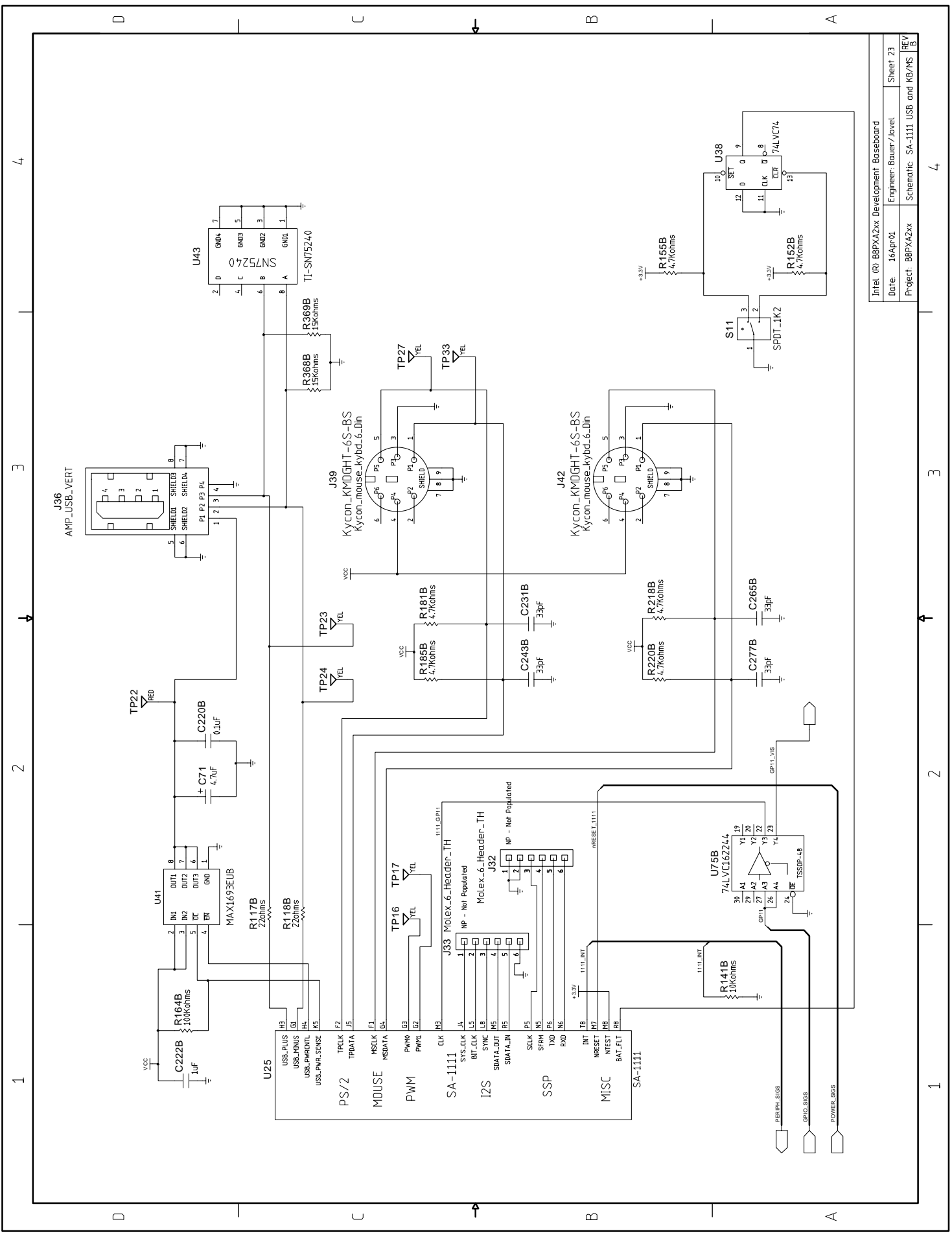


Intel (R) B8PXA2xx Development Baseboard		
Date:	16Apr01	Sheet 19
Project:	B8PXA2xx	Schematic: SP2_SPPROM
REV	B	

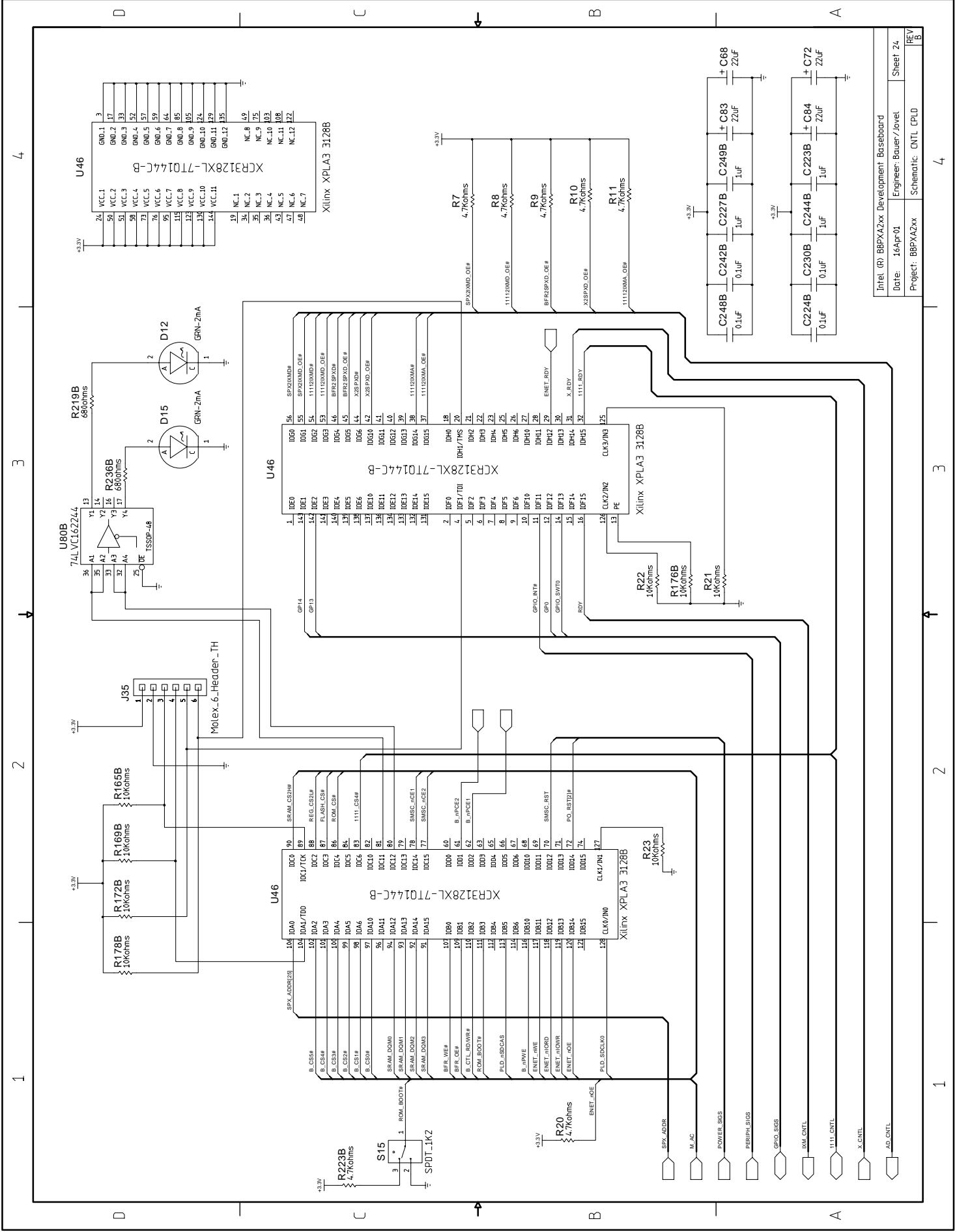


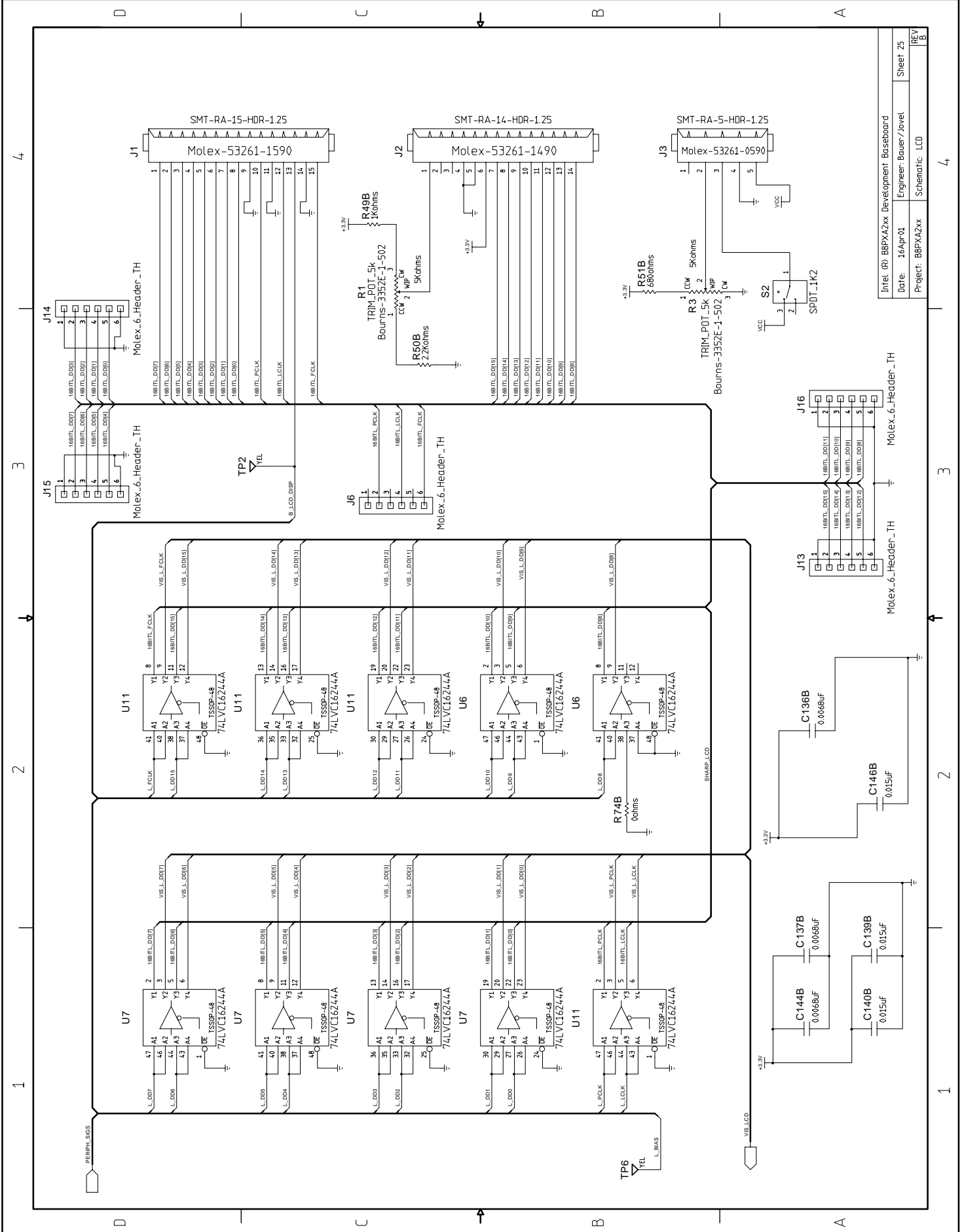


Intel (R) B8PXA2xx Development Baseboard		
Date: 16Apr01	Engineer: Bauer/Jovel	Sheet 22
Project: B8PXA2xx	Schematic: CF and P0MC0A PU	REV B

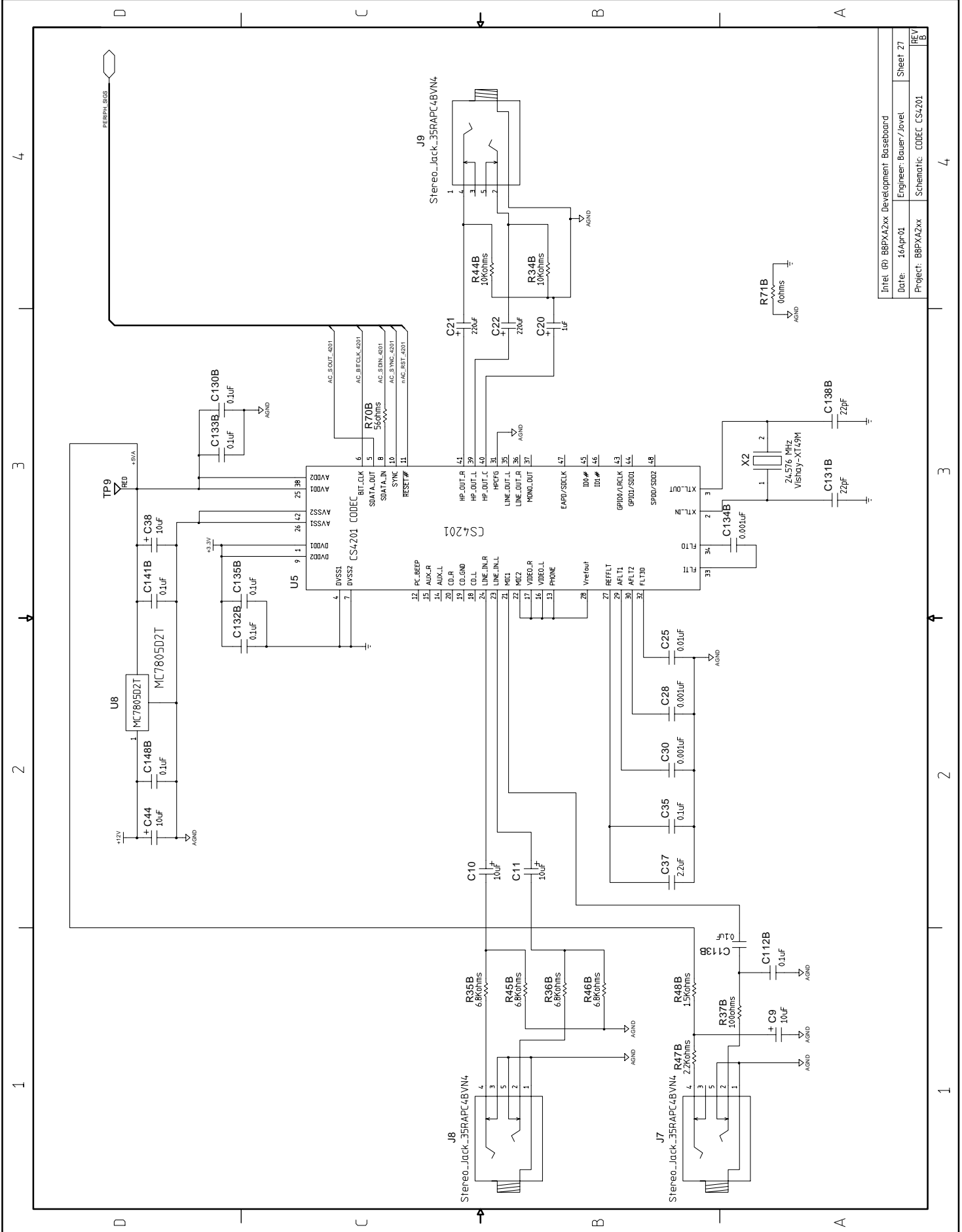


Intel (R) B8PXA2xx Development Baseboard			
Date:	16Apr01	Engineer:	Bauer/Jovel
Project:	B8PXA2xx	Schematic:	SA-1111 USB and KB/MS
		REV	B



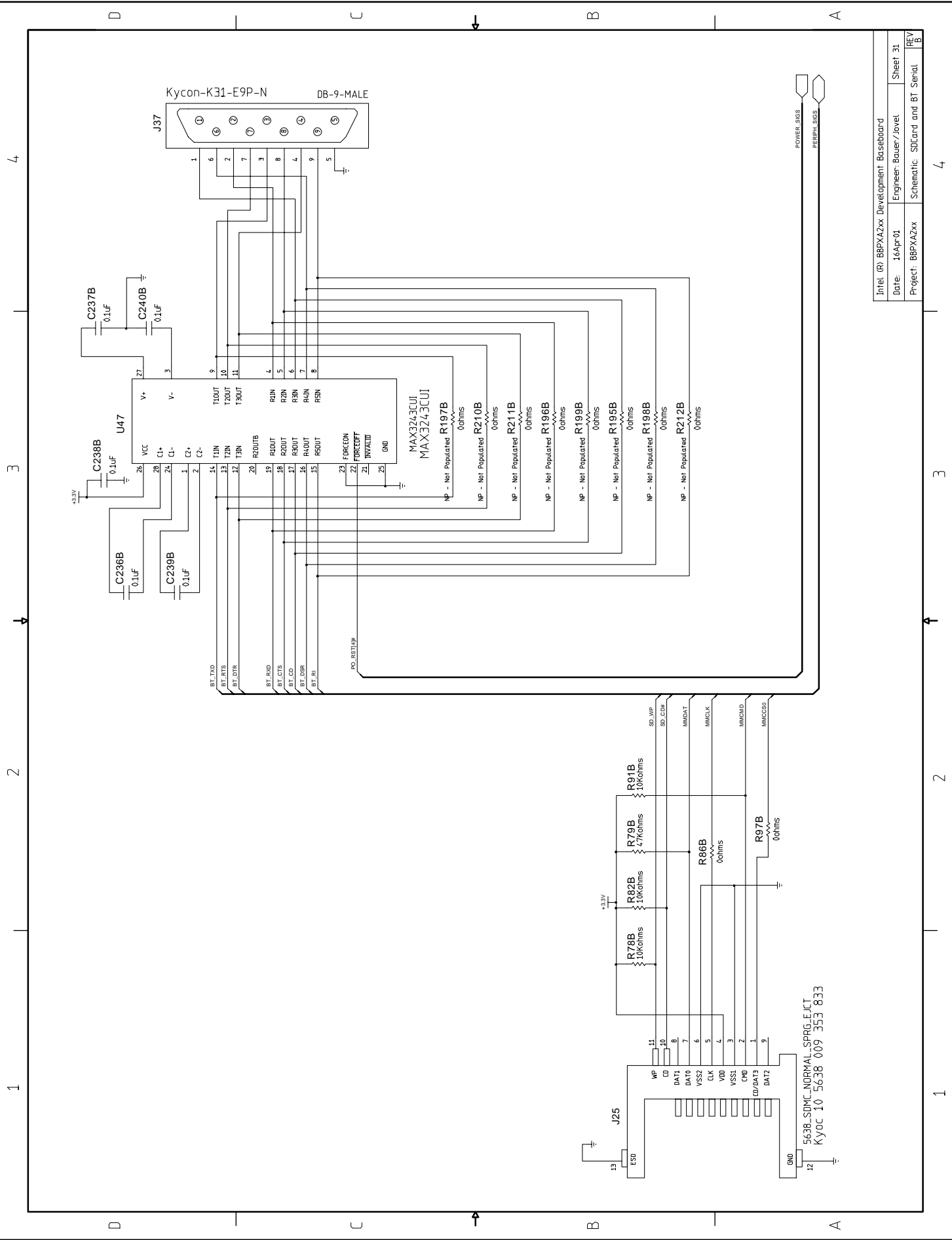


Intel (R) BBPXA2xx Development Baseboard	Sheet 25	REV B
Date: 16Apr01	Engineer: Bauer/Javel	
Project: BBPXA2xx	Schematic: LCD	

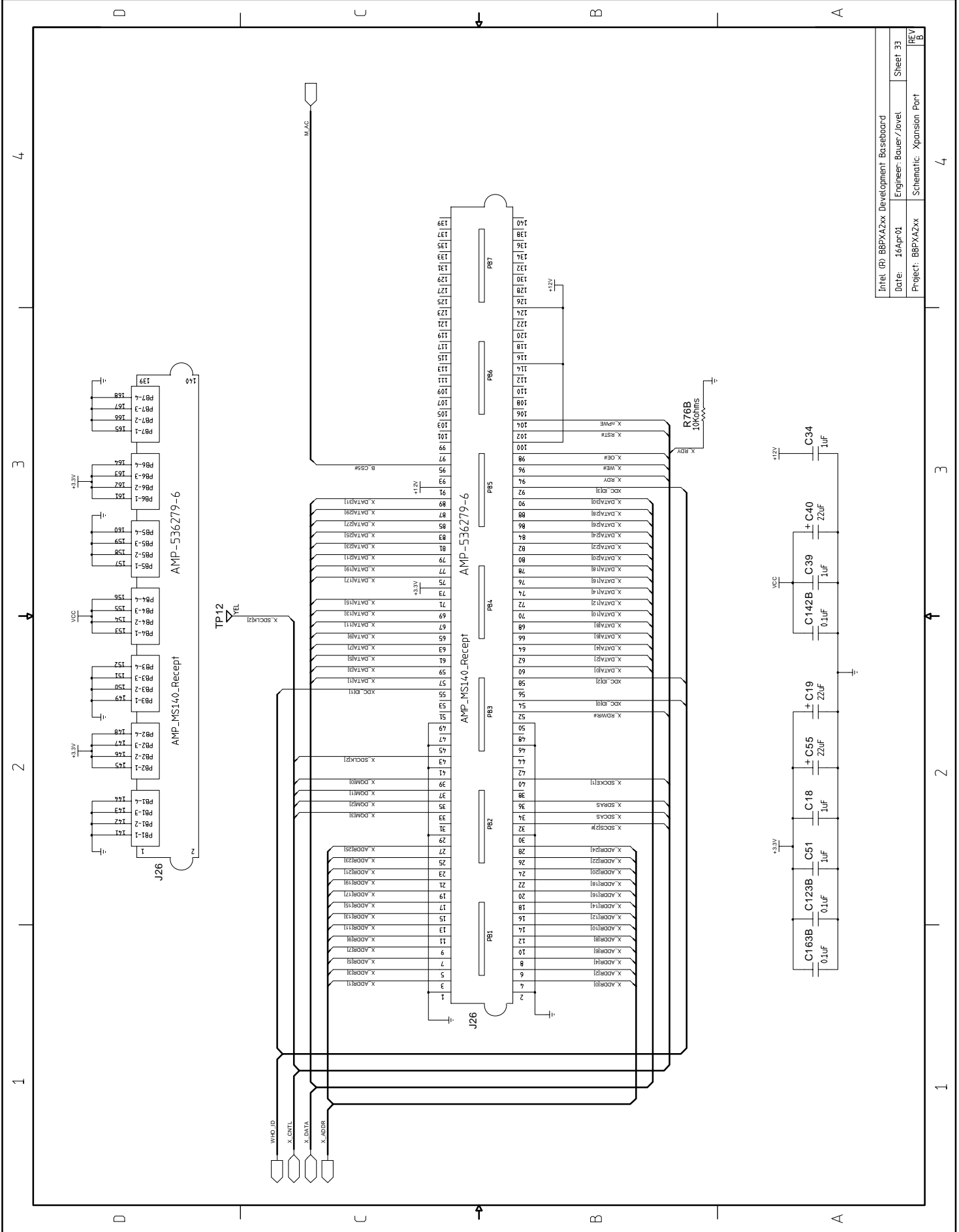


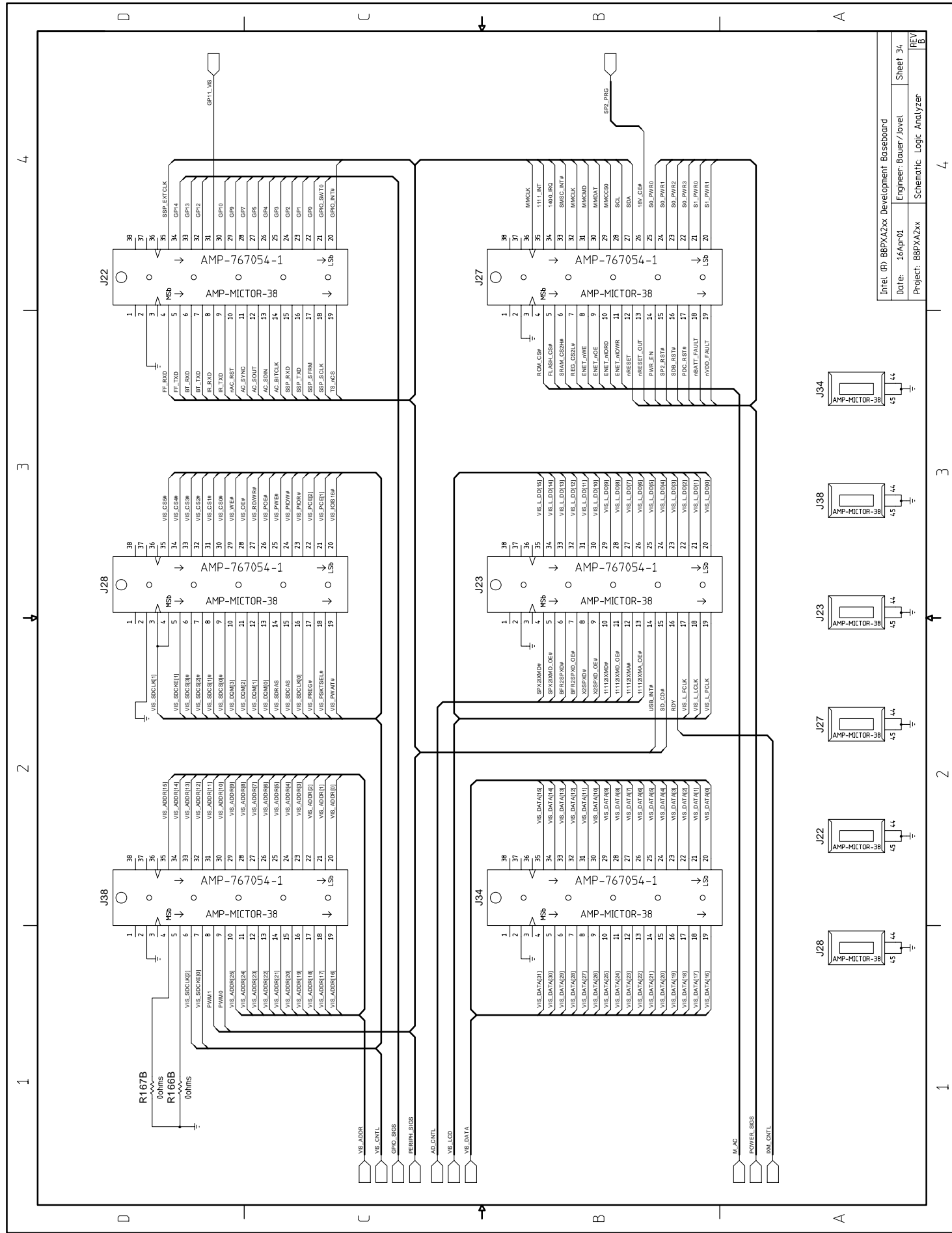
Intel (R) BBPXA2xx Development Baseboard			
Date:	16Apr01	Engineer:	Bauer/Jovel
Project:	BBPXA2xx	Schematic:	CODEC_CS4201
REV	B	Sheet	27

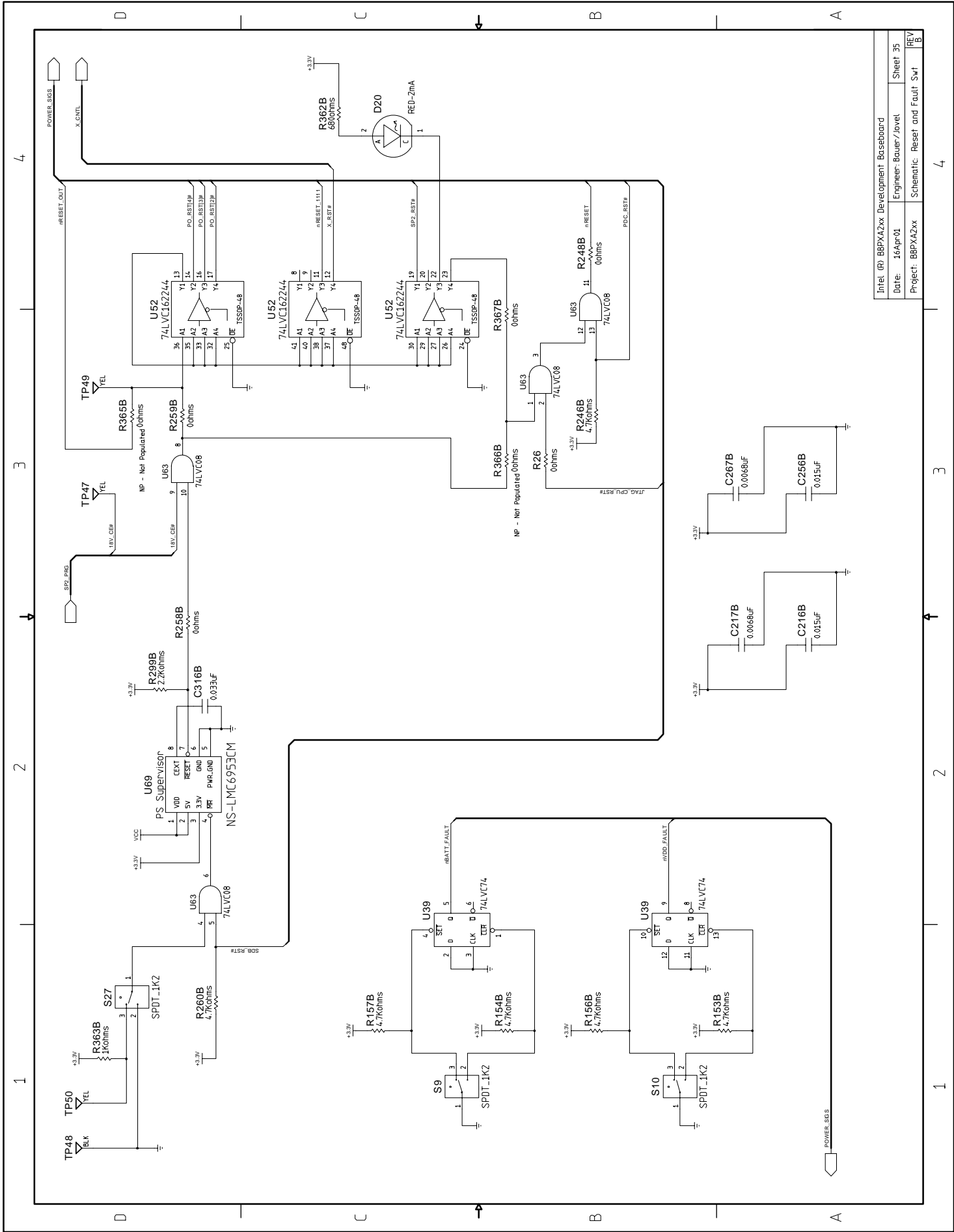


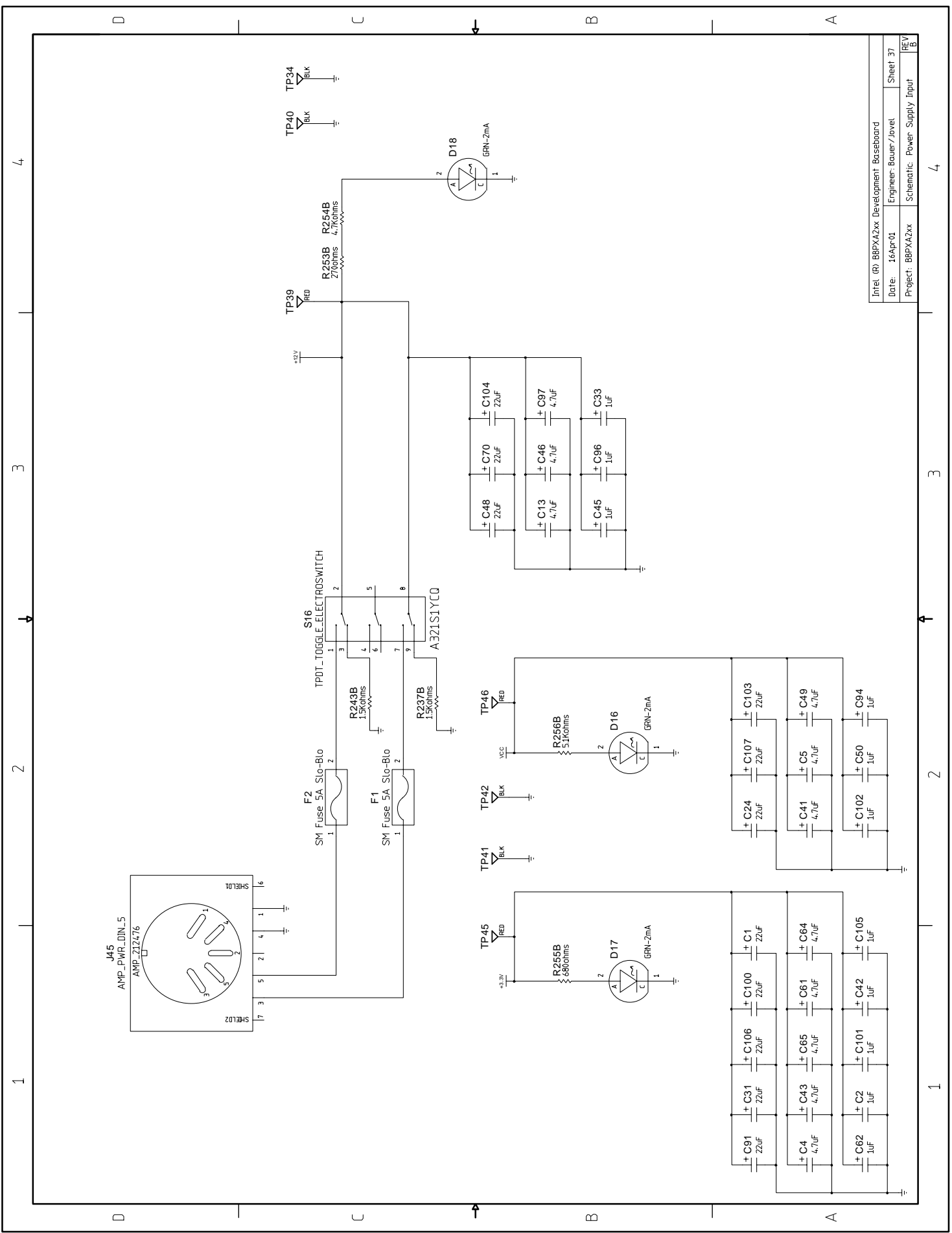


Intel (R) 88PXA2xx Development Baseboard	
Date: 16Apr'01	Engineer: Bauer/Jovel
Project: 88PXA2xx	Schematic: SDCard and BT Serial
REV B	
Sheet 31	

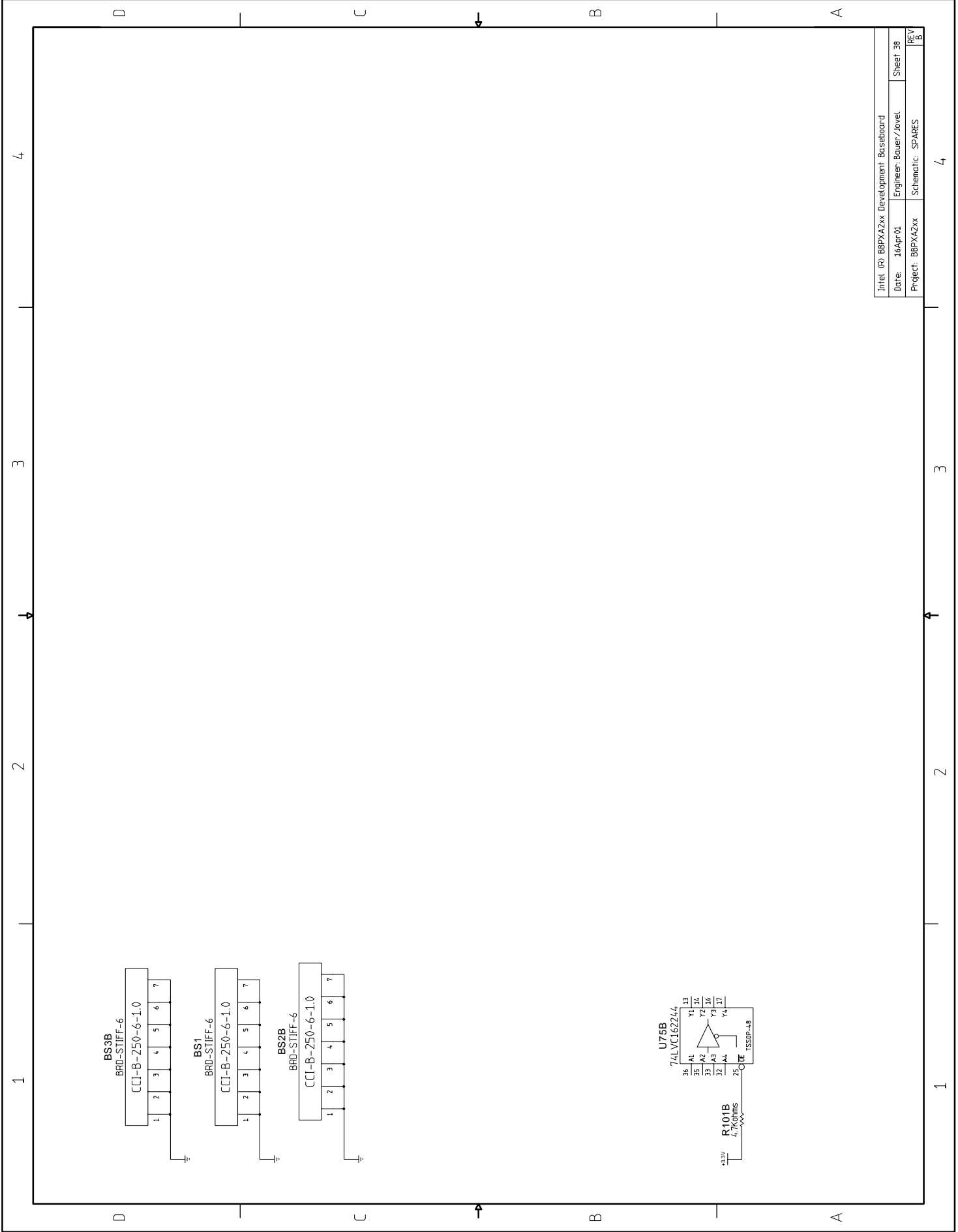








Intel (R) B8PXA2xx Development Baseboard		
Date:	16Apr'01	Sheet 37
Project:	B8PXA2xx	Schematic: Power Supply Input
REV	B	



Intel (R) B8PXA2xx Development Baseboard			
Date:	16Apr01	Engineer: Bauer/Jovel	Sheet: 38
Project:	B8PXA2xx	Schematic: SPARES	REV: B

Intel® BBPXA2xx Development Baseboard Rev (B - 002) Schematics Index

Format: Signal name followed by schematic sheet number (located in the lower right hand corner of each sheet) where each signal can be found

Netname	Sheet List	27	AGND	28	FWRPT#	13,14	HEX7[12]	14,15	MCMOD	31,34	50_CD1#	21,22	S1_PWR1	14,20,34	VIS_DOM[1]	8,34
+2.5V	19,30	B	AGND1		GND		HEX7[4]	14,15	MDCAT	31,34	S0_CD2#	21,22	S1_RSTST#	21,22	VIS_DOM[2]	8,34
+3.3V							HEX7[5]	14,15	M.AC	31,34	S0_CD2#	21,22	S1_RSTST#	21,22	VIS_DOM[3]	8,34
3.4,5,6,7,8,9,10,11,12,1							HEX7[6]	14,15	4	8,11,12,13,14,24,32,33,3	S0_CD2#	21,22	S1_VS2#	21,22	VIS_TOIS16#	25,34
3.14,15,							HEX8[0]	14,15	4	8,11,12,13,14,24,32,33,3	S0_D[0]	21,22	S1_VS2#	21,22	VIS_LCD	25,34
+5VA	27						HEX8[1]	14,15	N	30,34	S0_D[1]	21,22	S1_WAITH	21,22	VIS_L_DD[0:15]	25,34
+12V							HEX8[2]	14,15	DAC_RST	30,34	S0_D[2]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
20,27,30,33,36,37							HEX8[3]	14,15	DAC_RST_1400	28,30	S0_D[3]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[0]	25						HEX8[4]	14,15	DAC_RST_4201	27,30	S0_D[4]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[1]	25						HEX8[5]	14,15	16BATT_FAULT	34,35	S0_D[5]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[2]	25						HEX8[6]	14,15	RCG0	3,8	S0_D[6]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[3]	25						HEX8[7]	14,15	RCG1	3,8	S0_D[7]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[4]	25						HEX8[8]	14,15	RCG2	3,8	S0_D[8]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[5]	25						HEX8[9]	14,15	RCG3	3,8	S0_D[9]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[6]	25						HEX8[10]	14,15	RCG4	3,8	S0_D[10]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[7]	25						HEX8[11]	14,15	RCG5	3,8	S0_D[11]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[8]	25						HEX8[12]	14,15	RCG6	3,8	S0_D[12]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[9]	25						HEX8[13]	14,15	RCG7	3,8	S0_D[13]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[10]	25						HEX8[14]	14,15	RCG8	3,8	S0_D[14]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[11]	25						HEX8[15]	14,15	RCG9	3,8	S0_D[15]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[12]	25						HEX8[16]	14,15	RCG10	3,8	S0_D[16]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[13]	25						HEX8[17]	14,15	RCG11	3,8	S0_D[17]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[14]	25						HEX8[18]	14,15	RCG12	3,8	S0_D[18]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_DD[15]	25						HEX8[19]	14,15	RCG13	3,8	S0_D[19]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[20]	14,15	RCG14	3,8	S0_D[20]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[21]	14,15	RCG15	3,8	S0_D[21]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[22]	14,15	RCG16	3,8	S0_D[22]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[23]	14,15	RCG17	3,8	S0_D[23]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[24]	14,15	RCG18	3,8	S0_D[24]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[25]	14,15	RCG19	3,8	S0_D[25]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[26]	14,15	RCG20	3,8	S0_D[26]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[27]	14,15	RCG21	3,8	S0_D[27]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[28]	14,15	RCG22	3,8	S0_D[28]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[29]	14,15	RCG23	3,8	S0_D[29]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[30]	14,15	RCG24	3,8	S0_D[30]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[31]	14,15	RCG25	3,8	S0_D[31]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[32]	14,15	RCG26	3,8	S0_D[32]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[33]	14,15	RCG27	3,8	S0_D[33]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[34]	14,15	RCG28	3,8	S0_D[34]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[35]	14,15	RCG29	3,8	S0_D[35]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[36]	14,15	RCG30	3,8	S0_D[36]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[37]	14,15	RCG31	3,8	S0_D[37]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[38]	14,15	RCG32	3,8	S0_D[38]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[39]	14,15	RCG33	3,8	S0_D[39]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[40]	14,15	RCG34	3,8	S0_D[40]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[41]	14,15	RCG35	3,8	S0_D[41]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[42]	14,15	RCG36	3,8	S0_D[42]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[43]	14,15	RCG37	3,8	S0_D[43]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[44]	14,15	RCG38	3,8	S0_D[44]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[45]	14,15	RCG39	3,8	S0_D[45]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[46]	14,15	RCG40	3,8	S0_D[46]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[47]	14,15	RCG41	3,8	S0_D[47]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[48]	14,15	RCG42	3,8	S0_D[48]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[49]	14,15	RCG43	3,8	S0_D[49]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[50]	14,15	RCG44	3,8	S0_D[50]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[51]	14,15	RCG45	3,8	S0_D[51]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[52]	14,15	RCG46	3,8	S0_D[52]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[53]	14,15	RCG47	3,8	S0_D[53]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[54]	14,15	RCG48	3,8	S0_D[54]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[55]	14,15	RCG49	3,8	S0_D[55]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[56]	14,15	RCG50	3,8	S0_D[56]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[57]	14,15	RCG51	3,8	S0_D[57]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[58]	14,15	RCG52	3,8	S0_D[58]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[59]	14,15	RCG53	3,8	S0_D[59]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[60]	14,15	RCG54	3,8	S0_D[60]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[61]	14,15	RCG55	3,8	S0_D[61]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[62]	14,15	RCG56	3,8	S0_D[62]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[63]	14,15	RCG57	3,8	S0_D[63]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[64]	14,15	RCG58	3,8	S0_D[64]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[65]	14,15	RCG59	3,8	S0_D[65]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[66]	14,15	RCG60	3,8	S0_D[66]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[67]	14,15	RCG61	3,8	S0_D[67]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[68]	14,15	RCG62	3,8	S0_D[68]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[69]	14,15	RCG63	3,8	S0_D[69]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[70]	14,15	RCG64	3,8	S0_D[70]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[71]	14,15	RCG65	3,8	S0_D[71]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[72]	14,15	RCG66	3,8	S0_D[72]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[73]	14,15	RCG67	3,8	S0_D[73]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[74]	14,15	RCG68	3,8	S0_D[74]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[75]	14,15	RCG69	3,8	S0_D[75]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[76]	14,15	RCG70	3,8	S0_D[76]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[77]	14,15	RCG71	3,8	S0_D[77]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[78]	14,15	RCG72	3,8	S0_D[78]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[79]	14,15	RCG73	3,8	S0_D[79]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[80]	14,15	RCG74	3,8	S0_D[80]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[81]	14,15	RCG75	3,8	S0_D[81]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[82]	14,15	RCG76	3,8	S0_D[82]	21,22	S1_WAITH	21,22	VIS_L_FCLK	25,34
16BTLT_FCLK	25						HEX8[83]	14,15	RCG77	3,8	S0_D[83]					



PXA26x Processor Card Schematic Diagram

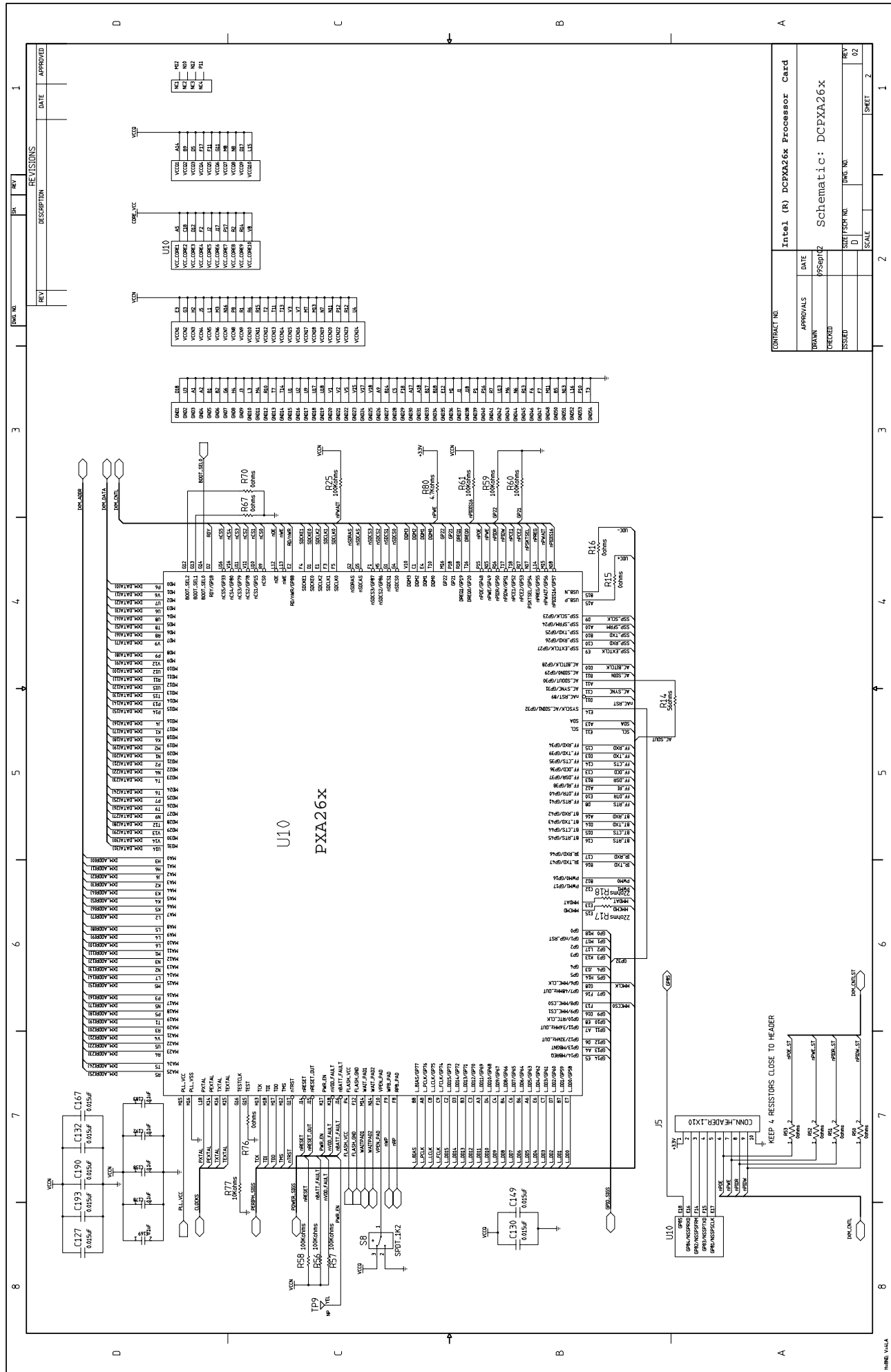
B

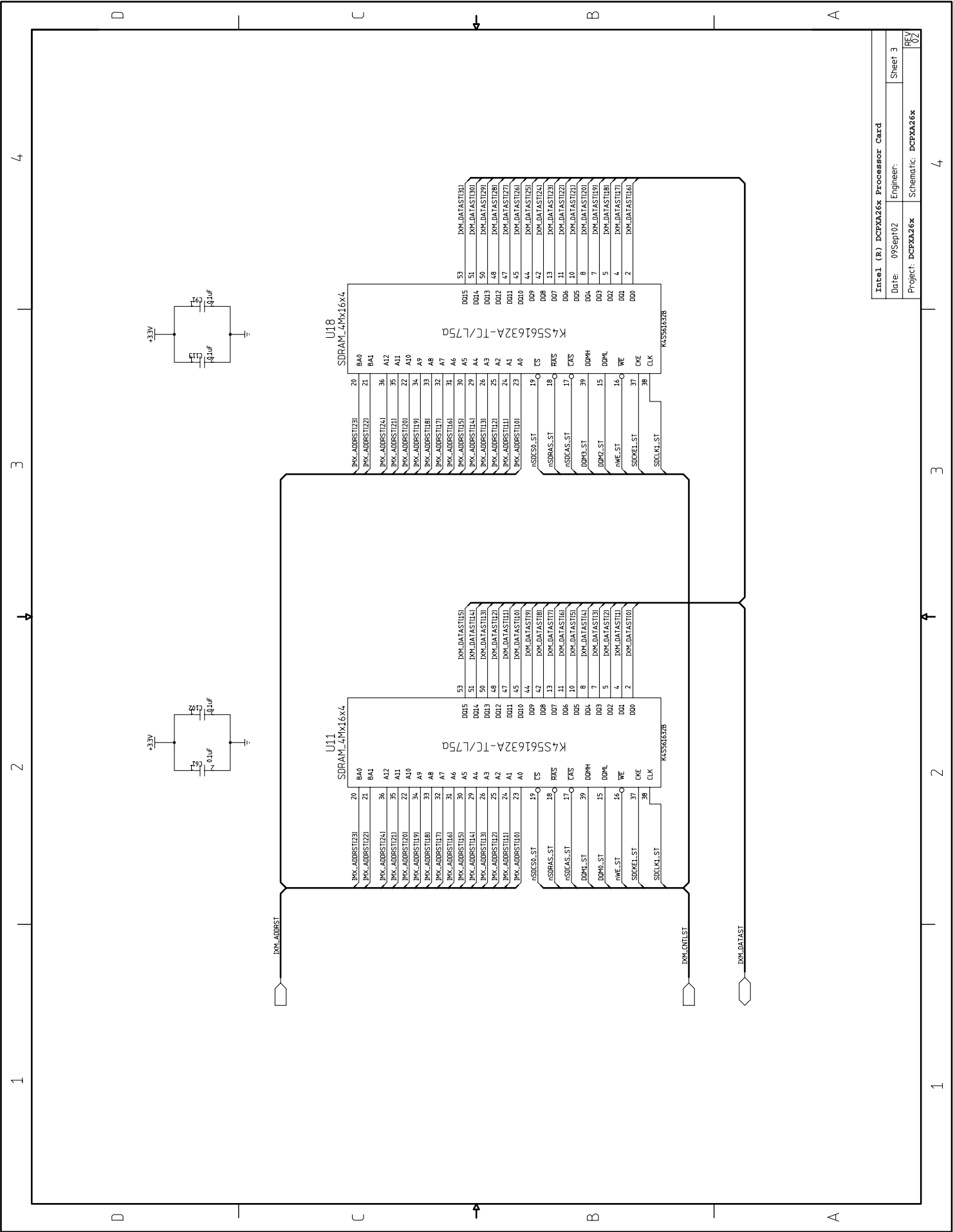
Intel(R) DCPXA26x Processor Card

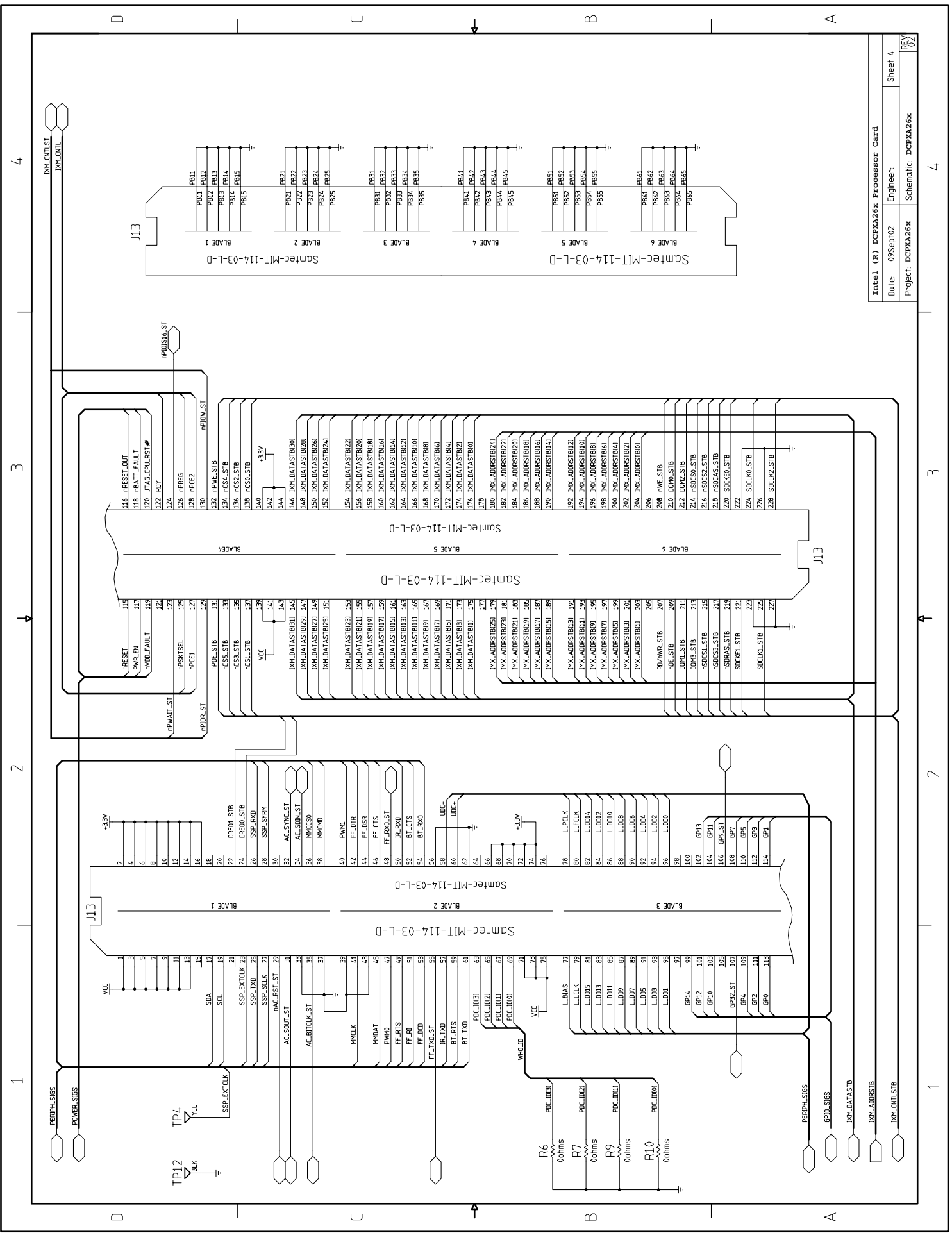
TABLE OF CONTENTS

PAGE	FUNCTION
1	TITLE PAGE
2	PROCESSOR --- PXA26x
3	SDRAM
4	CONNECTOR (MEMORY and I/O SIGNALS)
5	CLOCKS
6	JTAG CONNECTOR & PLL and CORE VOLTAGE REGULATORS
7	BYPASS CAPS
8-10	Bus Terminators
11-12	Data, Address and Control Transceivers
13	CPLD
14	TEST HEADERS

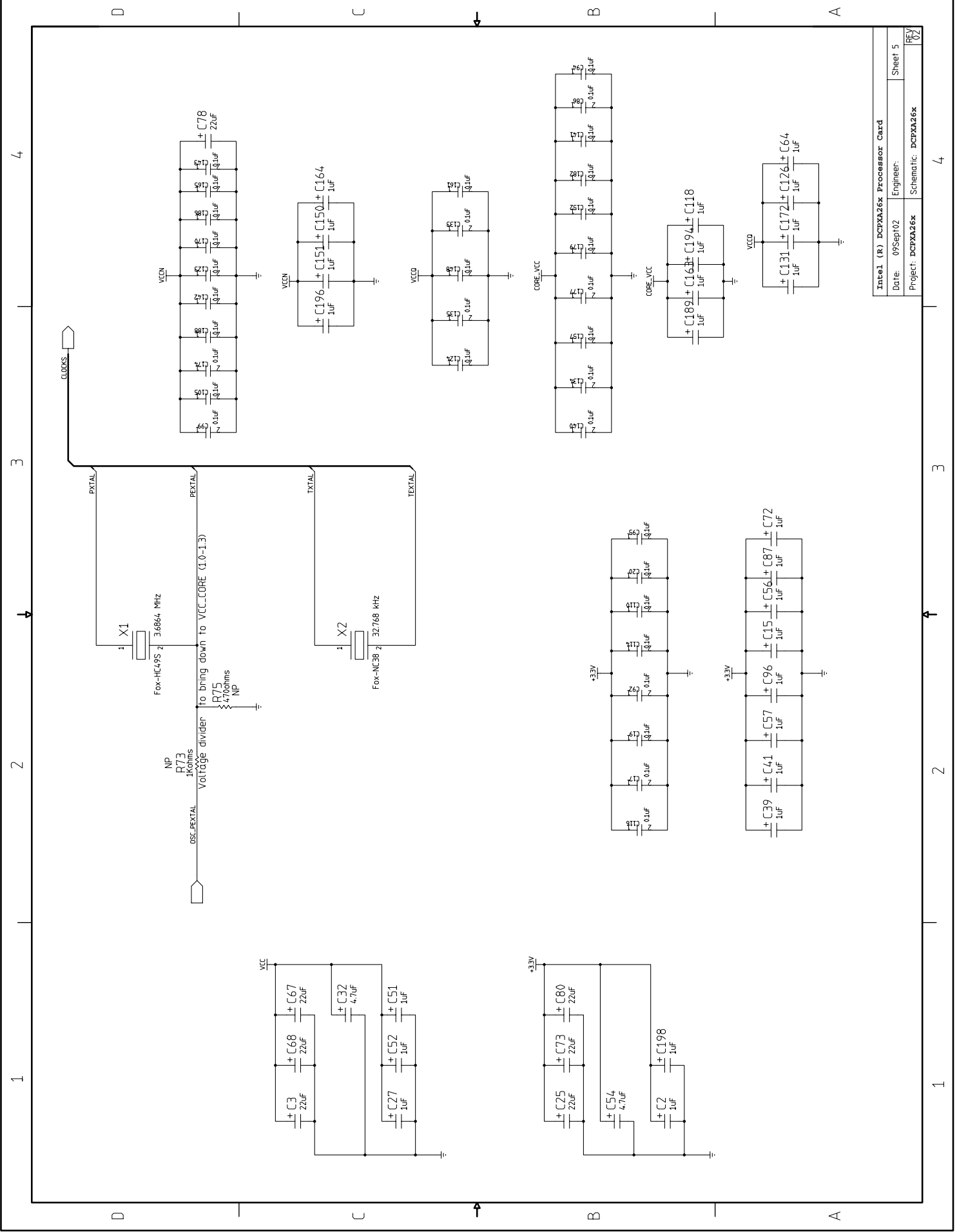
Intel (R) DCPXA26x Processor Card			
Date:	09Sept02	Engineer:	Sheet 1
Project:	DCPXA26x	Schematic:	DCPXA26x
REV	02		







Intel (R) DCPXA26x Processor Card		
Date: 09Sept02	Engineer:	Sheet 4
Project: DCPXA26x	Schematic: DCPXA26x	REV 02



Intel (R) DCPXA26x Processor Card		
Date:	09Sept02	Engineer:
Project:	DCPXA26x	Schematic: DCPXA26x
REV	02	



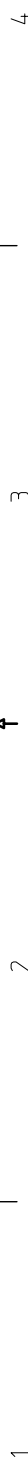
Downloaded from <http://ajphaphysocpharm.sagepub.com/> at 11:01 11 November 2014

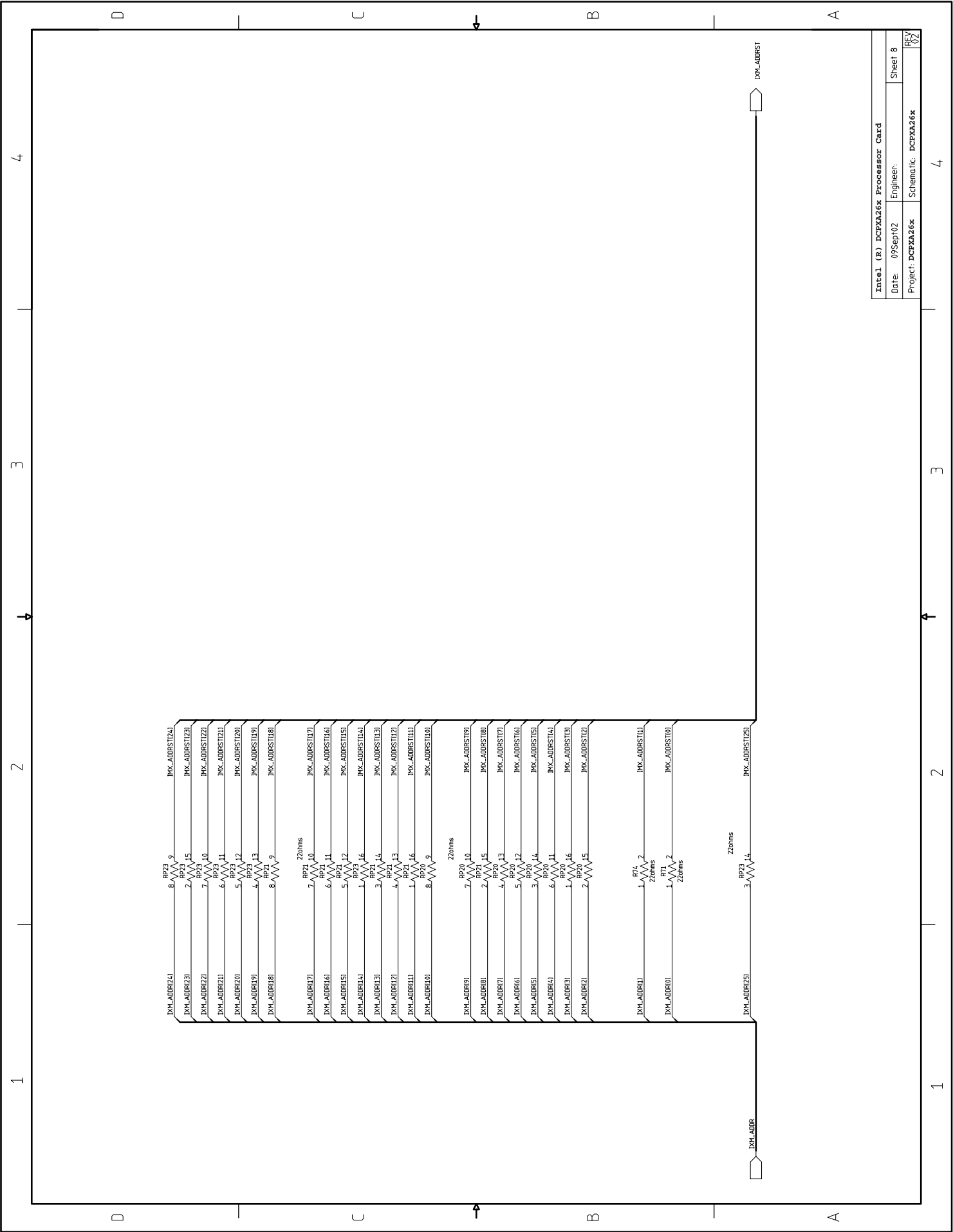


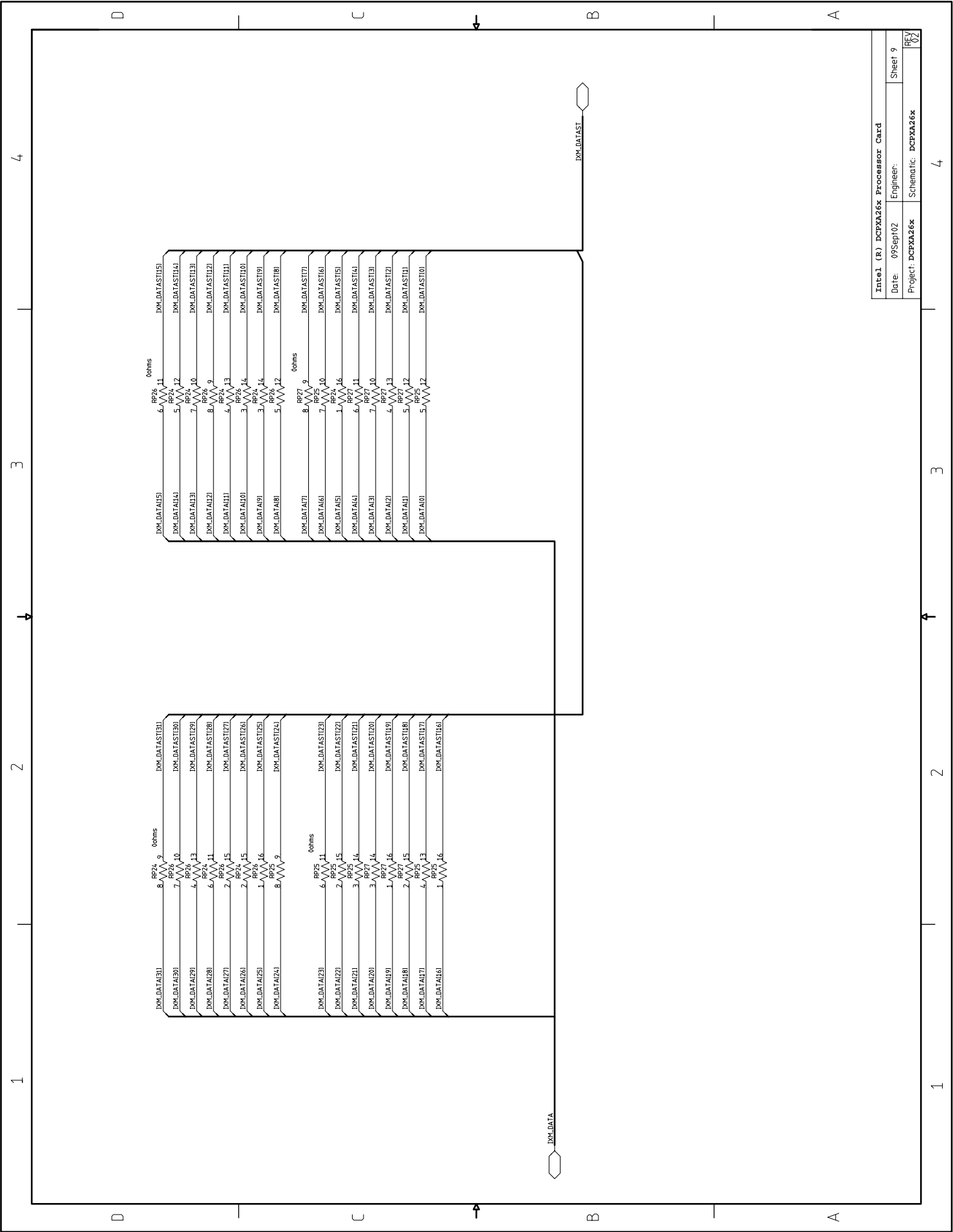
0.1 μ F



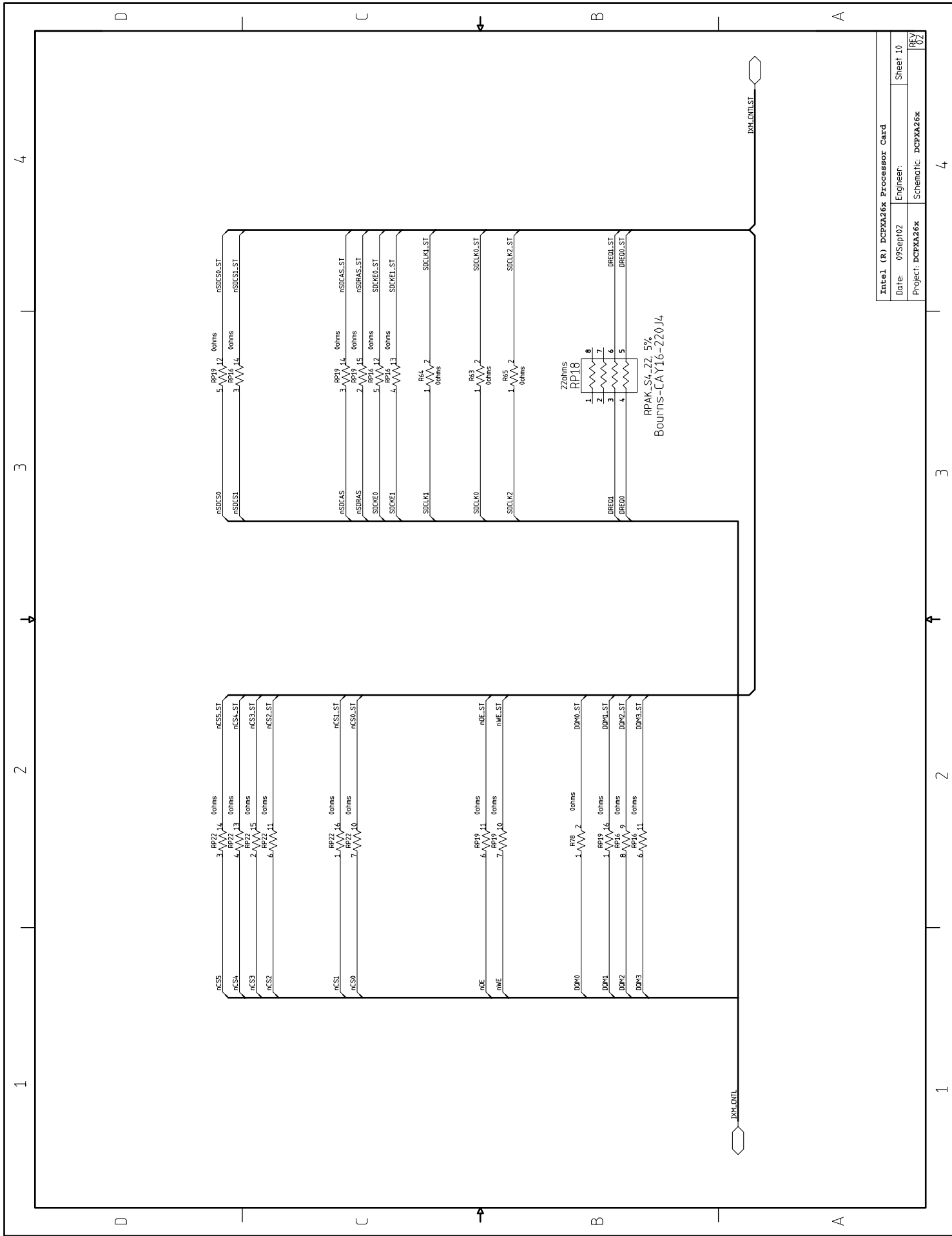
$$4, \cup^F \quad 4, \cap^F \quad 4, \cup^F \quad 4, \cap^F$$

REV





Intel (R) DCPXA26x Processor Card		
Date: 09Sept02	Engineer:	Sheet 9
Project: DCPXA26x	Schematic: DCPXA26x	REV 02



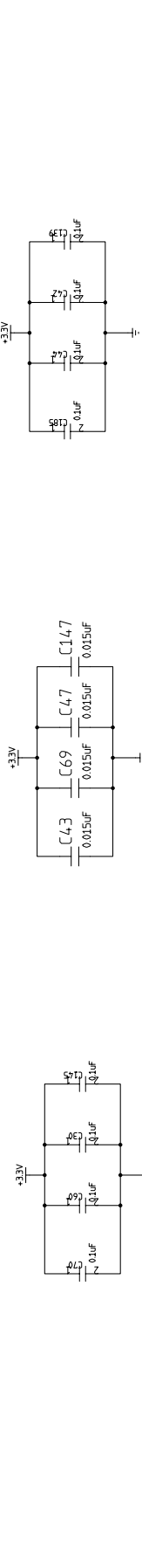
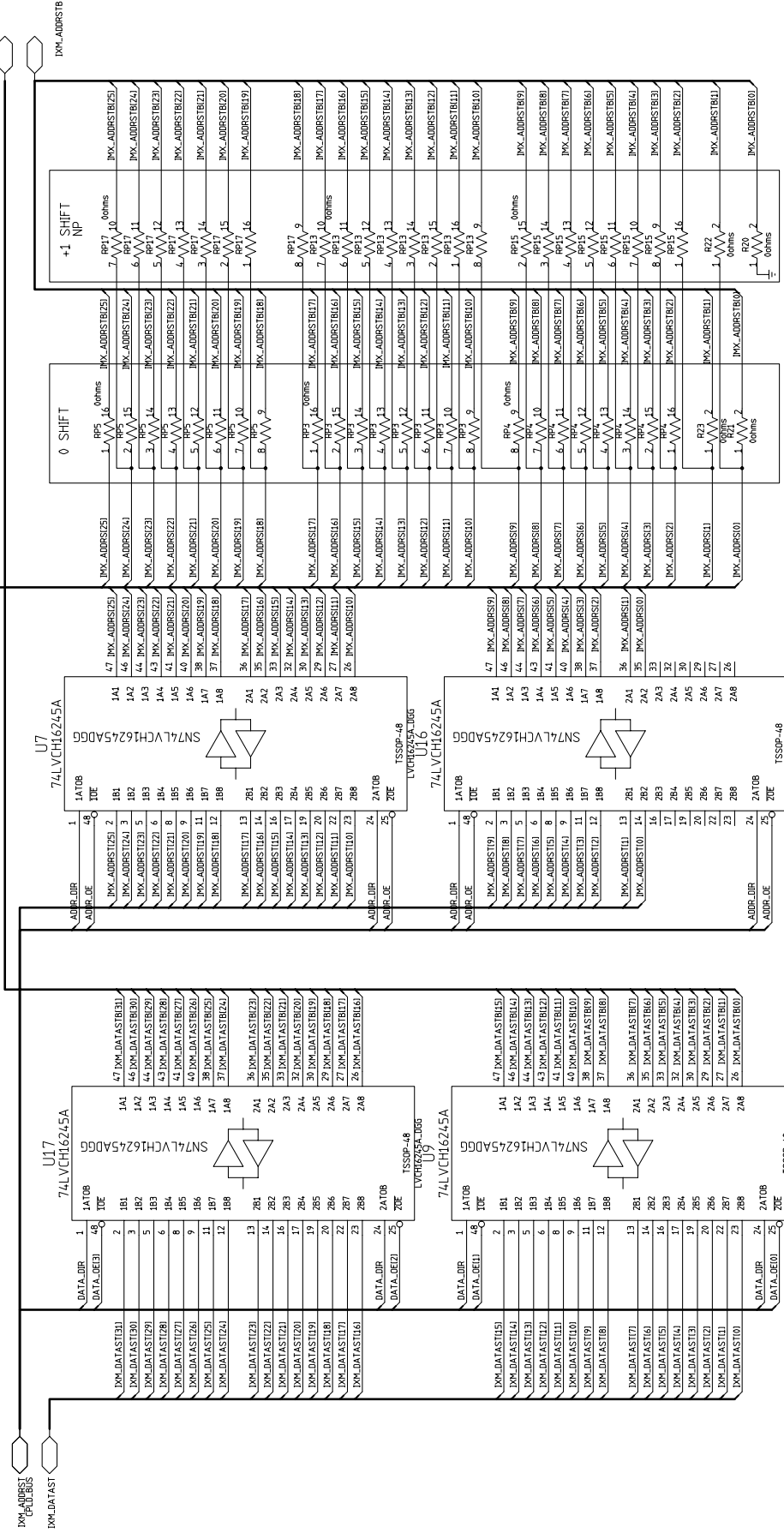
DATA BUFFERS ADDRESS BUFFERS ADDRESS SHIFT RESISTORS

DMX.DATASB

DMX.ADDRS

DMX.ADRSTB

DMX.ADRSTB



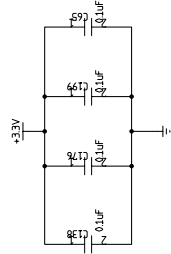
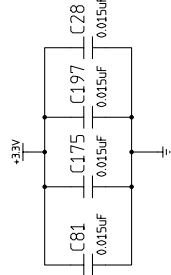
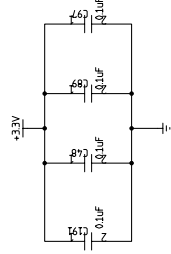
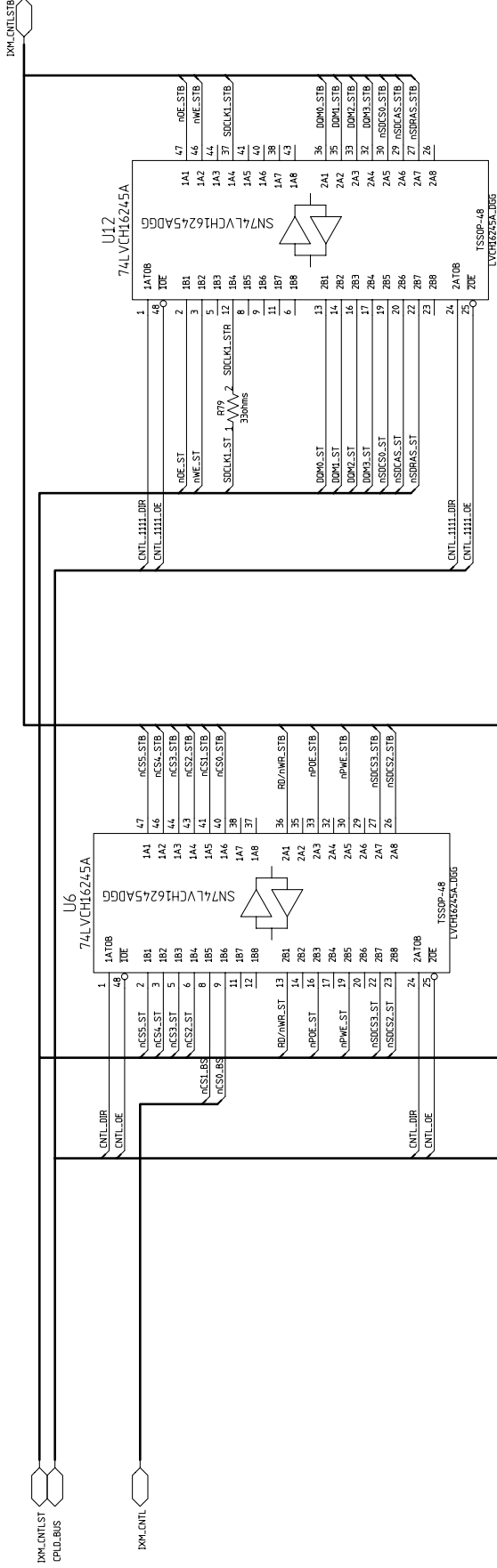
1

2

3

4

CONTROL BUFFERS



Intel (R) DCPXA26x Processor Card		
Date:	09Sept02	Engineer:
Project:	DCPXA26x	Schematic: DCPXA26x
REV	02	Sheet 12

1

2

3

4

