



Intel® PXA26x Processor Family

Specification Update

September 2003

Notice: The Intel® PXA26x Processor may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: **278641-008**

Intel Confidential



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

MPEG is an international standard for video compression/decompression promoted by ISO. Implementations of MPEG CODECs, or MPEG enabled platforms may require licenses from various entities, including Intel Corporation.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, 2003

AlertVIEW, i960, AnyPoint, AppChoice, BoardWatch, BunnyPeople, CablePort, Celeron, Chips, Commerce Cart, CT Connect, CT Media, Dialogic, DM3, EtherExpress, ETOX, FlashFile, GatherRound, i386, i486, iCat, iCOMP, Insight960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel ChatPad, Intel Create&Share, Intel Dot.Station, Intel GigaBlade, Intel InBusiness, Intel Inside, Intel Inside logo, Intel NetBurst, Intel NetStructure, Intel Play, Intel Play logo, Intel Pocket Concert, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel TeamStation, Intel WebOutfitter, Intel Xeon, Intel XScale, Itanium, JobAnalyst, LANDesk, LanRover, MCS, MMX, MMX logo, NetPort, NetportExpress, Optimizer logo, OverDrive, Paragon, PC Dads, PC Parents, Pentium, Pentium II Xeon, Pentium III Xeon, Performance at Your Command, ProShare, RemoteExpress, Screamline, Shiva, SmartDie, Solutions960, Sound Mark, StorageExpress, The Computer Inside, The Journey Inside, This Way In, TokenExpress, Trillium, Vivonic, and VTune are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.



Contents

Revision History 5

Preface..... 6

Summary of Changes 9

Errata 13

Specification Changes 23

Sleep Mode - Fast Sleep Wakeup 23

Specification Clarifications 27

Documentation Changes 28



Revision History

Revision Date	Version	Description
September 2003	-008	Added previous document changes Modified errata 32 Added errata 33
July 2003	-007	Added documentation change 1 , 7 , 8 (21, 22, 23)
May 2003	-006	Added documentation change 1 (20)
April 2003	-005	Added documentation changes 16, 17, 18, and 19 Added errata 33
March 2003	-004	Added errata 31 , 32 Added specification change 2 , 3 Added documentation change 9, 10, 11, 12, 13, 14, and 15
February 2003	-003	Added errata 25 , 26 , 27 , 28 , 29 , and 30 Added specification change 1 Added documentation changes 3, 4, 5, 6, 7, and 8
November 2002	-002	Added documentation change 1, 2
September 2002	-001	First publication

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

We have endeavored to include all documented errata in the consolidation process; however, we make no representations or warranties concerning the completeness of the Intel® PXA26x Processor Family Specification Update. This document may also contain information that was not previously published.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
<i>Intel® PXA26x Processor Family Developer's Manual</i>	278638
<i>Intel® PXA26x Processor Family Design Guide</i>	278639
<i>Intel® PXA26x Processor Family Electrical, Mechanical, and Thermal Specification</i>	278640

Nomenclature

Errata are design defects or errors. These may cause the Intel® PXA26x Processor Family's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices unless otherwise noted.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the document.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the document.

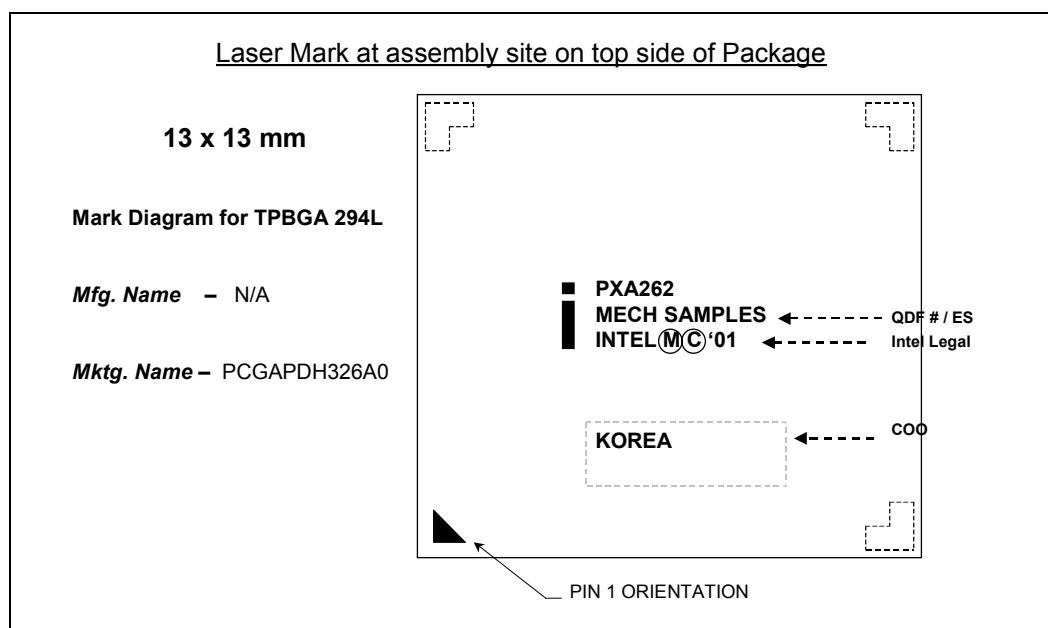
Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the document.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

General Information

PXA26x processor package markings are shown in [Table 1](#).

Figure 1. Package Markings



Summary of Changes

The following tables indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the PXA26x processor. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Doc:	Intel intends to update the appropriate documentation in a future revision.
Shaded:	This item is either new or modified from the previous version of the document.

Summary of Errata (Sheet 1 of 2)				
NO.	B0	Refer to:	Status	ERRATA
1	X	13	No Fix	"Multimediocard Stream Data Writes Do Not Transmit Properly"
2	X	13	No Fix	"Watchdog Reset Causes The Real Time Clock (RTC) To Increment At The Wrong Frequency"
3	X	13	No Fix	"Drain Write Buffer Command Does Not Force All Memory Requests Out To The External Bus"
4	X	14	No Fix	"Unindexed Mode LDC/STC Instructions Can Corrupt Protected Registers"
5	X	14	No Fix	"Aborted Store That Hits the Data Cache Marks Write-back Data Dirty"
6	X	14	No Fix	"MAC Instructions May Not Be Executed During Debug Mode"
7	X	14	No Fix	"A Load That Follows a DTLB Invalidate Entry Command Will Also Be Invalidated."
8	X	15	No Fix	"JTAG Highz Instruction Not 1149.1 Compliant"
9	X	15	No Fix	"Instruction Fetch Unit (IFU) Misses an External Abort"
10	X	15	No Fix	"SDRAM Auto Power Down Does Not Shut Off SDCLKs 0, 1, and 2 When Their Respective Partitions Are Not Being Accessed"
11	X	15	No Fix	"Memory Controller GPIO Pins Float High After Reset and Cause a Write to Address 0x0"
12	X	16	No Fix	"The SPI Protocol In The MMC Is Giving CRC Errors On Every Commands Response."
13	X	16	No Fix	"MMC Compatibility issue with different brand MMC cards."
14	X	16	No Fix	"MMC SPI mode – if card is deselected, PROG_DONE will not be set."
15	X	16	No Fix	"Long idle time on external bus between DREQ and nCS for flow-through DMA."
16	X	17	No Fix	"MMC – invalid data can be written to card if user stops then restarts the clock prior to end of data transfer."
17	X	17	No Fix	"PMU monitoring event #1, cycles in which the I-cache cannot deliver an instruction, is incorrectly incremented"
18	X	17	No Fix	"In Special Debug State, back to back memory transactions may hang if the first memory operation receives a precise data abort."
19	X	17	No Fix	"Certain frequency points are not supported."
20	X	18	No Fix	"Overflow on the Receive FIFO for the PCM channel of the AC97 unit will leave the FIFOs in an unrecoverable state."
21	X	18	No Fix	"SET_FEATURE/CLEAR_FEATURE Request with an illegal feature selector value will cause the UDC controller to respond incorrectly."

Summary of Errata (Sheet 2 of 2)				
NO.	B0	Refer to:	Status	ERRATA
22	X	18	No Fix	"The JTAG Controller must have the 3.6864 MHz oscillator running to work."
23	X	19	No Fix	"USB – Invalid value in EP0 Status Register if OPR bit is not cleared before the next SETUP packet."
24	X	19	No Fix	"DMA accesses to 8bit PCMCIA I/O space cause additional reads."
25	X	19	No Fix	"Indeterminate results may occur in certain peripherals during a frequency change if they are active"
26		20	Fixed	"GPIO wake-up event may be missed"
27		20	No Fix	"Slow IrDA Transmit pulse width cropped when SET BREAK is used"
28		20	Fixed	"Spurious Edge detects on GPIO pins can cause false Interrupts"
29		21	No Fix	"Fast Infrared FIR mode fails IrDA spec"
30		21	No Fix	"Asserting MBREQ during the MRS command transfer can cause SDRAM data corruption"
31		21	No Fix	"Invalid AC'97 interrupt during cold reset"
32		21	No Fix	"GPIO output signals, memory address pins and the memory controls pins, nOE and nWE, are unpredictable in sleep."
33		22	No Fix	"Non-branch instruction in vector table may execute twice after a thumb mode exception"

Summary of Specification Changes				
NO.	B0	Refer to:	Status	Specification Changes
1	X	23	Fixed	"New minimum spec for tD_NTRST and tD_NRESET"
2	X	23		"New Fast Wake from Sleep feature"
3	X	26	Fixed	"Voltage for low frequency range raised to 1.0V"

Summary of Specification Clarifications				
NO.	Document Revision	Refer to:	Status	Specification Clarifications
NOTE: There are no specification clarifications at this time.				

Summary of Documentation Changes				
NO.	Document Revision	Refer to:	Status	Documentation Changes
1	278638-002 Developer's Manual	28	Doc	"VLIO nOE/nPWE de-assertion time of RDN+1."
2	278638-002 Developer's Manual	28	Doc	"VLIO nOE/nPWE de-assertion time of RDN+1 for Figure 6-18 and 6-19."
3	278638-002 Developer's Manual	28	Doc	"VLIO nOE/nPWE de-assertion time of RDN+1 for Table 6-22."
4	278638-002 Developer's Manual	29	Doc	"VLIO nOE/nPWE de-assertion time of RDN+1 for Table 6-21."
5	278638-002 Developer's Manual	29	Doc	"Table 3-1: Core PLL Output Frequencies for 3.6864 MHz Crystal"
6	278638-002 Developer's Manual	30	Doc	"Table 12-13: UDC Control Function Register"
7	278638-002 Developer's Manual	32	Doc	"Update to Register Table 12-33 at end of Chapter 12."
8	278638-002 Developer's Manual	33	Doc	"Update to Table 2-8 at end of Chapter 2 System Architecture"

Errata

1. Multimediacard Stream Data Writes Do Not Transmit Properly

Problem: MultiMediaCard stream data writes of length equal to $(n*32)+6$ bytes, where $n=1,2,3,\text{etc.}$, do not transmit properly. The MMC card does not receive one of the bytes but it does receive the stop command.

Implication: When the MMC unit transmits $(n*32)+6$ bytes, the MMC card actually receives $(n*32)+5$ bytes. It is impossible to determine which byte is missing.

Workaround: Driver software must break up stream data writes equal to $(n*32)+6$ bytes into separate transactions that are not equal to $(n*32)+6$.

Status: No Fix

2. Watchdog Reset Causes The Real Time Clock (RTC) To Increment At The Wrong Frequency

Problem: When a watchdog reset occurs, the internal logic that uses the RTC Trim Register (RTTR) values to set the frequency of the RTC become out of sync and no longer increment the RTC at the correct frequency.

Implication: The RTC clock value (RCNR) becomes invalid because the RTC no longer increments at the correct frequency after watchdog resets.

Workaround: After every watchdog reset:

- If the lock bit is not set in the RTTR register, write the appropriate value to the RTTR register and then write the appropriate value to the RCNR register.
- If the lock bit is set in the RTTR register, do a dummy write to the RTTR register to resync the internal logic to the original RTTR value that was written before the lock bit was set, and then write the appropriate value to the RCNR register.

Status: No Fix

3. Drain Write Buffer Command Does Not Force All Memory Requests Out To The External Bus

Problem: Whether there are outstanding memory requests in the execution pipeline or not the drain write buffer command does not correctly force all outstanding memory requests completely out to the external bus.

Implication:

Workaround: Two workarounds are available to ensure a write propagates out to the external bus.

- Perform a read back from the same location that just written to.
- Perform any transaction to a memory page marked $X=C=B=0$ (IO cycle).

Both workarounds ensure all previous memory transactions complete before execution begins on any subsequent instructions.

Status: No Fix

4. **Unindexed Mode LDC/STC Instructions Can Corrupt Protected Registers**

Problem: Unindexed mode LDC or unindexed mode STC can corrupt protected registers.

Implication: This error can be seen in any of the following scenarios:

- During the execution of an LDC instruction, FIQ mode registers r8-r14 and debug mode register r13 could be corrupted
- During the execution of an STC instruction, Rn could be corrupted
- Memory locations could be corrupted based on the base register

Workaround: Do not use unindexed addressing for LDC or STC instructions

Status: No Fix

5. **Aborted Store That Hits the Data Cache Marks Write-back Data Dirty**

Problem: An aborted store that hits in the data cache does not modify the contents of the data cache but the dirty bit for that cache line is set.

Implication: If there is no other external bus master in the system that will be sharing memory regions with the processor, this erratum will simply write-back data out to external memory, even though the data really was not modified. In normal operation this will be nothing more than an extra store on the bus that writes the same data to memory that is already there.

If another bus master in the system exists, this erratum manifests itself in the following manner. The processor loads in a cache line from a memory region shared with another bus master. The external bus master modifies the same line in external shared memory. The processor attempts to modify data in the cache line, hits the cache, aborts because of MMU permissions, the data is not modified, but sends the dirty bit. When the cache line is evicted, the original data overwrites any data written by the external bus master.

Workaround: Use one of the following suggestions:

- Mark shared memory as write-through
- Use semaphores
- Use other handshaking techniques to prevent collisions on shared memory

Status: No Fix

6. **MAC Instructions May Not Be Executed During Debug Mode**

Problem: MAC instructions may not be executed during debug mode. When the processor goes into the debug handler and enters a special debug state, MAC instructions are not executed if another exception occurs. The debug handler does not have any indication that the MAC instruction did not execute.

Implication: The accumulator does not update properly or have the correct value because the MAC instruction does not execute.

Workaround: Disable debug in the Debug Control and Status Register (DCSR) before doing a MAC instruction.

Status: No Fix

7. **A Load That Follows a DTLB Invalidate Entry Command Will Also Be Invalidated.**

Problem: If a load or store instruction immediately follows an Invalidate Data Translation Look-aside Buffer (DTLB) Entry command (mcr p15, 0, Rd, c8, c6, 1) and the page table entry required by the load/store instruction is resident in the data TLB, the load/store entry will be invalidated along with the

target of the Invalidate D-TLB entry command. This can also occur if one instruction with an issue latency of one cycle is executed after the Invalidate D-TLB entry command and before the load/store instruction.

Implication:

Workaround: Follow all DTLB Invalidate Entry commands with two no-ops.

Status: No Fix

8. JTAG Highz Instruction Not 1149.1 Compliant

Problem: JTAG HIGHZ instruction is not IEEE 1149.1 compliant.

Implication: The processor violates the IEEE 1149.1 specification because it places the outputs into an inactive state one clock after the HIGHZ instruction.

Workaround: Insert an extra clock after the HIGHZ instruction to three-state the pads.

Status: No Fix

9. Instruction Fetch Unit (IFU) Misses an External Abort

Problem: If a bus abort occurs on a code fetch while a Instruction Translation Look-aside Buffer (I-TLB) lock instruction is outstanding, the IFU fails to abort. Instead, the IFU will execute the instruction returned on the aborting transaction. This problem does not affect parity errors.

Implication:

Workaround: Execute the instruction Sub pc, pc #4 after every I-TLB or I-Cache lock command. The Sub pc, pc #4 instruction is not predicted, which causes the pipeline to be flushed.

Status: No Fix

10. SDRAM Auto Power Down Does Not Shut Off SDCLKs 0, 1, and 2 When Their Respective Partitions Are Not Being Accessed

Problem: If MDREFR[APD] is set, the processor does not shut off the appropriate SDCLKs when their respective partitions are not being accessed. This causes no functional problems.

Implication: When the core accesses any SDRAM partition, all SDCLKs (i.e., SDCLK<2:0>) come on, and all SDCLKs stay on until the core does not need to access any of the SDRAM partitions.

Workaround: None

Status: No Fix

11. Memory Controller GPIO Pins Float High After Reset and Cause a Write to Address 0x0

Problem: When a hard reset occurs, the address bus is driven to 0x0. If a hard reset is asserted during a static chip select write cycle, the address bus is driven to 0x0 quickly but nCSx and nWE return to the de-asserted state more slowly which means a write to address 0x0 can occur. This is evident with all static memory devices, PCMCIA, and CF.

Implication: If a hard reset is asserted, the address bus is 0x0 while the chip select pin and write enable pin is still asserted. Any data at address 0x0 could be overwritten with random data.

Workaround: None

Status: No Fix

12. The SPI Protocol In The MMC Is Giving CRC Errors On Every Commands Response.

Problem: If the cyclic redundancy check (CRC) enable bit is set in the SPI register while using the SPI protocol, the MMC controller gives a false "CRC error on response" to every command it sends out. If this CRC error is ignored, the data transfers correctly and there is no CRC error.

Implication:

Workaround: Ignore the CRC error during the command response period.

Status: No Fix

13. MMC Compatibility issue with different brand MMC cards.

Problem: The X means that the card is compatible in that mode.

Card					
Mode		Lexar	Sandisk	Viking	DaneElec
	SPI	X		X	X
	Stream		X		
	Block	X	X	X	X

In stream mode the last 2 bytes are read as zeros in rest of the three cards (other than Sandisk)

Stream mode on Sandisk is seeing an underrun error being returned from the card at the 4 highest speeds. All the rest of the speeds (5 – 7) are functional.

Implication:

Workaround:

Status: No Fix

14. MMC SPI mode – if card is deselected, PROG_DONE will not be set.

Problem: If changing SPI chip selects, the PROG_DONE bit does not get updated with the state of the selected card.

Implication: If programming card0, then switch to card1, then come back to card0, there is no way of knowing if card0 ever finished programming

Workaround: User can tie MMDAT signal to a GPIO and monitor the signal by reading the GPIO status register until the signal goes high.

Status: No Fix

15. Long idle time on external bus between DREQ and nCS for flow-through DMA.

Problem: While observing a flow through DMA transaction, DREQ is asserted, then traffic on the SDRAM bus finishes, then there is approximately 500ns (50 SDCLKs) of no activity before the chip select associated with the DMA is asserted. This only occurs once in many DMA transactions.

The problem was that the internal bus arbiter was being retried due to internal buffers being full. This retry was taking an excessive amount of time.

Implication:

Workaround:

Status: No Fix

16. MMC – invalid data can be written to card if user stops then restarts the clock prior to end of data transfer.

Problem: For block writes (single and multiple) it was found that if the user stops the clock and restarts it, say with a CMD12 programmed to stop the data transfer, the MMC can send out bad data to the card.

This only applies to the case where the clock is stopped/started by writing to the MMC_STRPCL register, not when the MMC controller stops/starts the clock based on whether the TX fifo has data in it.

The data corruption does not apply to stream mode writes.

Implication: There is no guarantee of the data transfers, response contents, etc. if software turns the clock off before a command and data sequence is complete.

Workaround: Software should never turn the clock off before the end of a command protocol and any data transfer, with the exception of the stop command for stream writes.

Status: No Fix

17. PMU monitoring event #1, cycles in which the I-cache cannot deliver an instruction, is incorrectly incremented

Problem: The only clock cycles that should be counted for PMU monitoring event #1 are for I-cache misses or I-TLB misses. Many other events may erroneously cause this counter to increment.

Implication:

Workaround: Do not use PMU monitoring event #1.

Status: No Fix

18. In Special Debug State, back to back memory transactions may hang if the first memory operation receives a precise data abort.

Problem: Special Debug State (SDS) is used by debug vendors. If a back to back store is used in SDS, and the first store receives a precise data abort, the first memory operation is correctly cancelled, but the second memory operation may leave the core in an unknown state.

Implication:

Workaround: While in SDS, any memory operation that may cause a precise data abort must be followed by a Drain Write Buffer command. Load Multiple/Store Multiple that may cause precise data aborts must not be used.

Status: No Fix

19. Certain frequency points are not supported.

Problem: The device does not support the listed frequency points:

Turbo Mode Frequency	Run Mode Frequency	PXbus Frequency	Mem, LCD Frequency	SDRAM Frequency
235.9	118.0	59	118.0	59
235.9	235.9	118	118	59
353.9	118.0	59	118.0	59
132.7	132.7	66	132.7	66

Turbo Mode Frequency	Run Mode Frequency	PXbus Frequency	Mem, LCD Frequency	SDRAM Frequency
265.4	132.7	66	132.7	66
265.4	265.4	132.7	132.7	66
398.1	132.7	66	132.7	66
294.9	147.5	74	147.5	74
294.9	294.9	147.5	147.5	74
331.8	165.9	83	165.9	83

Implication:

Workaround:

Status: No Fix

20. **Overflow on the Receive FIFO for the PCM channel of the AC97 unit will leave the FIFOs in an unrecoverable state.**

Problem: If a receive overrun occurs on the AC97 Two-channel composite PCM Receive FIFO, this will stop the channel. The overrun can cause the most significant and least significant 16 bits of the FIFO (i.e. the left channel and right channel) to be switched. If the DMA or core later empties the FIFO, then this switching of data, and therefore invalid data, will continue to occur until the AC97 unit and the FIFO pointers are reset.

Implication: Software should assume that any overrun condition is fatal and that, following the error, the FIFO contents are invalid.

Workaround: If software wishes to manually stop the DMA that services the AC97 Receive FIFO, then first power off the ADC subsystem of the codec, then stop the DMA channel associated with the Receive FIFO. If done quickly enough (8 sample times, 166us at 48kHz), this should avoid the possibility of the Receive FIFO overflow and thus the Left/Right channel swapping.

If an overrun occurs on the AC97 Receive FIFO, and a Receive FIFO Overflow error in the PCM_In Status Register is indicated, then stop the DMA channel associated with the Receive FIFO, and issue a cold reset to the AC97 circuitry and to the AC97 unit, by setting GCR[COLD_RST] to zero.

Status: No Fix

21. **SET_FEATURE/CLEAR_FEATURE Request with an illegal feature selector value will cause the UDC controller to respond incorrectly.**

Problem: If the USB host issues a SET/CLEAR feature request with an illegal feature selector value, the UDC controller incorrectly responds to the request with an ACK handshake. The device should respond with a STALL.

Implication: Violates the USB 1.1 protocol since the UDC controller responds with an ACK rather than a STALL handshake to the USB host.

Workaround:

Status: No Fix

22. **The JTAG Controller must have the 3.6864 MHz oscillator running to work.**

Problem: The 3.6864 MHz on-chip oscillator must be running, either from a 3.6864 MHz crystal source or from a 3.6864 MHz clock source, in order for the JTAG Controller to work properly.

Implication: The JTAG Controller will not work with just a TCK clock source.

Workaround: The 3.6864 MHz on-chip oscillator must be running, either from a 3.6864 MHz crystal source or from a 3.6864 MHz clock source, in order for the JTAG Controller to work properly.

Status: No Fix

23. USB – Invalid value in EP0 Status Register if OPR bit is not cleared before the next SETUP packet.

Problem: After the Status-OUT stage of a USB Standard Control Read Command, such as GET_DESCRIPTOR, GET_CONFIGURATION, GET_INTERFACE, and GET_STATUS, if the user does not clear the UDCCS0[OPR] before the next SETUP packet is received, then the UDCCS0 could contain an invalid value.

The invalid value is UDCCS0 = 0x81, which indicates that a SETUP packet was received, but the UDDR0 Data FIFO is empty, however, the SETUP packet data is actually in the UDDR0 Data FIFO.

Implication: Software can get confused if the status register indicates that a SETUP packet was received (UDCCS0[SA]=1), an OUT packet is ready (UDCCS0[OPR]=1), but the UDDR0 Data FIFO is empty (UDCCS0[RNE]=0).

Workaround: Software should treat UDCCS0 = 0x81 as a valid value and read 8 bytes from the UDDR0 Data FIFO while ignoring UDCCS0[RNE]. This 8 bytes of data will be the correct data from the SETUP command.

Status: No Fix

24. DMA accesses to 8bit PCMCIA I/O space cause additional reads.

Problem: If DMA is used to access 8bit PCMCIA I/O space, additional reads can be generated if the length in the descriptor is odd.

Implication:

Workaround: Do not use DMA to access to 8bit PCMCIA I/O space. If DMA is used, software must ensure that the descriptor lengths are even.

Status: No Fix

25. Indeterminate results may occur in certain peripherals during a frequency change if they are active

Problem: Indeterminate results may occur in certain peripherals while transmitting or receiving data during a frequency change sequence.

Implication:

Workaround: If the operation of these peripherals would be adversely affected, then these peripherals would have to be disabled during a frequency change.

- MMC
- FFUART
- STUART
- BTUART
- IrDA
- SSP
- UDC
- AC97

Status: No Fix

26. GPIO wake-up event may be missed

Problem: While executing the sleep mode sequence after the write to CP14, as documented in page 3-16 of the *Intel® PXA26x Processor Family Developer's Manual*, there is a window of time which allows a GPIO wake-up to be completely ignored.

Implication: Wake-up events during this time period are completely missed.

Workaround: Do not use a single edge transition as a wake-up source. Instead use a pulse with a minimum width of three 32 KHz (93.75 μ S) clock cycles wide and setup the GPIO wake-up source pin to cause wake-up events with both the Rising Edge Detect Enable Register (GRER) and Falling Edge Detect Enable Register (GFER) enabled. Another alternative workaround is to use logic to hold off wake-up edge from the time the software decides to go to sleep until 93.75 μ S after the processor has entered sleep.

Status: Fixed

27. Slow IrDA Transmit pulse width cropped when SET BREAK is used

Problem: The Slow IrDA (SIR) port can show errors while transmitting data.

Implication: When the UART is transmitting in SIR mode, a cropped pulse can occur when the set break (SB) bit in the Line Control Register (LCR) is deasserted. This can occur in either XMODE 0 or XMODE 1 and at any baud rate. A pulse width as low as 0.8 μ S has been seen instead of the expected 1.6 μ S XMODE=1 pulse.

Workaround: Ensure that software does not attempt to disable the transmitter SIR enable bit (XMITIR) in the Infrared Selection Register (IRDASEL) and that LCR[SB] is not used while in SIR mode.

Status: No Fix

28. Spurious Edge detects on GPIO pins can cause false Interrupts

Problem: During heavy system bus traffic, spurious edge detects can occur.

Implication: All GPIO pins and GPIO alternate functions are susceptible to spurious edge detects causing Interrupts and external DMA requests (DREQs) to be incorrectly serviced. The DREQs are alternate function 1 of GPIO 19 and 20. The alternate functions are programmed by the GPIO Alternate Function Register (GAFR).

The following GPIOs are most affected by this issue: GPIOs 10, 11, 12, 13, 14, 15, 19, 20, 28, 31, 41, 78, 79 and 80, however GPIO 10 and 14 are affected more often.

Workaround: There is no known workaround for this errata. However, there are some guidelines to minimize the effects of this errata. These guidelines are listed below.

- Designing systems and software to distinguish between legitimate interrupts and spurious interrupts. A device status register can often be used by interrupt service routines to distinguish between a real interrupt and a false interrupt.
- Decreasing either VCCQ or VCCN voltages depending upon whether the spurious edges are seen on a GPIO (VCCQ) or an alternate function which is powered from VCCN.
- Increasing the VCC core voltage.
- Ensuring that the system has good decoupling such as 5 to 8, 0.015 μ F capacitors and 5 to 8, 0.1 μ F capacitors on both VCCN and VCCQ.

Status: Fixed

29. Fast Infrared FIR mode fails IrDA spec

Problem: The IR specification states that fast infrared FIR 4 Mbits/Sec operates at 8 MHz and has a rate tolerance of .01%. The processor has an FIR frequency of 7.98716 MHz which is an error rate of 0.16% which exceeds the IrDA Serial Infrared Physical Layer Specification, Version 1.4, February 6, 2001.

Implication: Systems using FIR mode will not be operating within Version 1.4 of the IrDA Serial Infrared Physical Layer Specification.

Workaround: Replace the 3.6864 MHz crystal with a 3.69 MHz crystal. This crystal frequency change enables the FIR mode of the processor to operate within specification.

Note: Changing the crystal, changes the base frequency to the clock manager and all of the peripherals. Ensure that complete system regression tests are used to validate the workaround.

Status: No Fix

30. Asserting MBREQ during the MRS command transfer can cause SDRAM data corruption

Problem: When the companion chip asserts the memory bus request MBREQ signal immediately after deassertion (such as, for a second time) which then occurs at the same time the Mode Register Set (MRS) command is sent to the SDRAM to configure them back to burst of 4, a data corruption of the SDRAM data is possible. This only occurs if the processor is in SA-1111 compatibility mode.

Implication: When the companion chip has control of the bus for SDRAM chip select 0, the SDRAM chip selects 1, 2, and 3 are held in their active low state until the companion chip releases control of the bus. If they exist, there is a potential for data corruption in the upper three banks of SDRAM.

Workaround: To avoid SDRAM data corruption, do not re-assert MBREQ for at least 80 memory clocks after the de-assertion of the previous MBREQ.

Status: No Fix

31. Invalid AC'97 interrupt during cold reset

Problem: Invalid AC'97 interrupt may occur when the 'cold reset' bit is set or cleared in the GCR.

Implication: A spurious interrupt may occur during a cold reset.

Workaround: Disable AC'97 interrupts before doing a cold reset by setting GCR[COLD_RST]. When the cold reset event is complete, the interrupts can be re-enabled.

Status: No Fix

32. GPIO output signals, memory address pins and the memory controls pins, nOE and nWE, are unpredictable in sleep.

Problem: When the PXbus frequency is greater than 133MHz, the states of the GPIO output signals, address pins and the memory control pins, nOE and nWE, are unpredictable in sleep.

Implication: When the PXbus frequency is greater than 133MHz,

- 1) GPIO signals that are configured as outputs may float.
- 2) If the FS bit in the PCFR register is set, nOE and nWE may not float during sleep.
- 3) The address bus pins MA[18:0] may attempt to return to their state for the last transaction.

Depending on how these signals are implemented in a system, this may result in increased power consumption.

Workaround: To drive or float these signals as documented during sleep, do a frequency change sequence (FCS) to a PXbus frequency of 133MHz or less. When the FCS is complete, the CCCR register can be set back to the original value before entering sleep. This will allow the processor to resume at the original frequency upon sleep wakeup.

To ensure that the GPIO signals maintain the correct state during sleep, the PGSR registers must be written with the correct values. This applies to all GPIO pins including those being used as alternate functions.

To prevent any affected address pins from changing state from low to high during sleep, the last instruction before the write to the co-processor putting the part to sleep should be a read from address 0x0.

Status: No Fix

33. Non-branch instruction in vector table may execute twice after a thumb mode exception

Problem: If an exception occurs in thumb mode and a non-branch instruction is executed at the corresponding exception vector, that instruction may execute twice.

Implication: Typically instructions located at exception vectors must be branch instructions which go to the appropriate handler, but the ARM architecture allows the FIQ handler to be placed directly at the FIQ vector (0x0000001c/0xffff001c) without requiring a branch. Because of this bug, the first instruction of such an FIQ handler may be executed twice if it is not a branch instruction.

Workaround: If a no-op is placed at the beginning of the FIQ handler, the no-op will execute twice and no incorrect behavior will result. If a branch instruction is placed at the beginning of the handler, it will not be executed twice.

Status: No Fix

Specification Changes

S1. New minimum spec for tD_NTRST and tD_NRESET

Problem: In Table 6-2 Power-On Timing Specifications of the *Intel® PXA26x Processor Family Electrical, Mechanical, and Thermal Specification* states:

tD_NTRST	Delay between VCC, PLL_VCC stable and nTRST deasserted	50	—	—	ms
tD_NRESET	Delay between VCC, PLL_VCC stable and nRESET deasserted	50	—	—	ms

Implication: The minimum times have been reduced allowing nRESET and nTRST to assert faster.

Workaround: Change the minimum specification for tD_NTRST and tD_NRESET in Table 6-2 Power-On Timing Specifications from 50ms to 10ms as shown below:

tD_NTRST	Delay between VCC, PLL_VCC stable and nTRST deasserted	10	—	—	ms
tD_NRESET	Delay between VCC, PLL_VCC stable and nRESET deasserted	10	—	—	ms

Note: tD_NTRST and tD_NRESET is the time from the last stable power supply.

Status: Fixed

S2. New Fast Wake from Sleep feature

Issue: The PXA26x Revision B1 adds support for Fast Wake from Sleep. Add the following sections to the Clocks and Power Manager section of the *Intel® PXA26x Processor Family Developer's Manual*:

3.4.8 Sleep Mode - Fast Sleep Wakeup

Sleep mode offers lower power consumption at the expense of the loss of most of the internal processor state. In sleep mode, the processor goes through an orderly shut-down sequence. The PXA26x processor supports two sleep mode configurations: one that minimizes power consumption and one that minimizes sleep exit latency.

To minimize power consumption during sleep, the VCC and PLL_VCC supplies must be driven to ground during sleep when PWR_EN deasserts. To minimize sleep exit latency, the VCC and PLL_VCC power supplies must remain enabled during sleep and software must disable the power supply stabilization delay during the wakeup sequence.

When in sleep mode, the power manager watches for a wake-up event and, after it receives one, re-establishes power (if needed) and goes through a reset sequence. During sleep mode, the RTC and power manager continue to function. Pin states can be controlled throughout sleep mode and external SDRAM is preserved because it is in self-refresh mode.

Because all activity on the processor except the RTC stops when sleep mode starts, peripherals must be disabled to allow an orderly shutdown. When sleep mode exits, the processor's state resets and processing resumes in a boot-up mode.

3.4.8.1 Sleep Mode External Voltage Regulator Requirements

For maximum flexibility with the implementation of sleep mode, the external power supply system must have these characteristics:

- A power enable input pin that enables the primary supply output connected to VCC and PLL_VCC. This pin must be connected to the processor's PWR_EN pin. To support fast sleep wakeup by maintaining power during sleep, the regulator should be software configurable to ignore PWR_EN. When PWR_EN is not used, VCC and PLL_VCC may be powered on before or simultaneously with VCCN and VCCQ. In this configuration, when PWR_EN is deasserted the core regulator must be able to maintain regulation when the load power is as little as 0.5 mW. Core supply current during sleep will vary with voltage and temperature.
- When core power is enabled during sleep, the power management IC or logic that generates nVDD_FAULT must assert this signal when any supply including VCC and PLL_VCC falls below the lower regulation limit during sleep. nVDD_FAULT must not be deasserted until all supplies are in regulation again since there is no power supply stabilization delay during the fast sleep wakeup sequence. If nVDD_FAULT is asserted during fast sleep wakeup, then the processor returns to sleep mode.
- When configured to disable the supply to save power during sleep, the core regulator's output must be driven to ground when PWR_EN goes low.
- Higher-voltage outputs connected to VCCQ and VCCN are continuously driven and do not change when the PWR_EN pin is asserted.

3.4.8.2 Preparing for Sleep Mode

Before sleep mode starts, software must take these steps:

1. The memory controller must be configured to ensure SDRAM contents are maintained during sleep mode. See Chapter 6, "Memory Controller" of the *Intel® PXA26x Processor Family Developer's Manual* for details.
2. If a graceful shutdown is required for a peripheral, the peripheral must be disabled before sleep mode asserts. This includes monitoring DMA transfers to and from peripherals or memories to ensure they are completed. All other peripherals need not be disabled, since they are held in their reset states internally during sleep mode.
3. The following power manager (PM) registers must be set up for proper sleep entry and exit:
 - PM GPIO Sleep State registers (PGSR0, PGSR1, PGSR2). To avoid contention on the bus when the processor attempts to wake up, ensure that the chip selects are not set to 0 during sleep mode. If a GPIO is used as an input, it must not be allowed to float during sleep mode. The GPIO can be pulled up or down externally or changed to an output and driven with the unasserted value.
 - PM General Configuration Register Float bits [FS/FP] must be configured appropriately for the system. The General Configuration Register Float bits must be cleared on wake up. To avoid contention on the bus when the processor attempts to wake up, ensure that the chip selects are not set to 0 during sleep mode. The PCFR[OPDE] bit must be cleared to leave the 3.6864 MHz enabled during sleep if the fast wakeup sleep configuration is selected by setting the PMFW[Fwake] bit.

- PMFW configuration register must be set to select between the standard and fast sleep wakeup configurations. Set PMFW[FWAKE] to 1 to disable the 10 ms power supply stabilization delay during sleep wakeup if power is maintained during sleep. This configuration reduces the sleep wakeup time to approximately 650 μ s.
- 4. Before the IDAE bit is set, software must configure an imprecise data abort exception handler to put the processor into sleep mode when a data abort occurs in response to nVDD_FAULT or nBATT_FAULT assertion. This abort exception event indicates that the processor is in peril of losing its main power supply.
- 5. These power manager registers must be set up to detect wake-up sources and oscillator activity:
 - PM GPIO Sleep State registers (PGSR0, PGSR,1 and PGSR2).
 - PM Wake-up Enable register (PWER)
 - PM GPIO Falling-edge Detect Enable and PM GPIO Rising-edge Detect Enable registers (PFER and PRER)
 - OPDE bit in the Power Manager Configuration Register (PCFR)
 - IDAE bit in PMCR

Note: The PCFR[OPDE] bit must be cleared to enable the 3.6864 MHz oscillator during sleep when fast sleep wakeup is selected by setting the PMFW[FWAKE] bit.

3.4.9 Power Manager Fast Sleep Wakeup Configuration Register (PMFW)

Table 2. PMFW Register Bitmap and Bit Definitions

0x40F0 0034										Power Manager Fast Sleep Wakeup Configuration Register (PMFW)										Power Manager												
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																FWAKE		Reserved													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31:3]	—		Reserved Read undefined and must always be written with zeroes.																													
[1]	FWAKE		FAST WAKEUP ENABLE 0 – Selects the standard sleep wakeup sequence with a 10 ms power supply stabilization delay when power is disabled during sleep. 1 – Selects the fast sleep wakeup sequence without a power supply stabilization delay when power is maintained during sleep. Cleared by hardware reset.																													
[0]	—		Reserved Read undefined and must always be written with zeroes.																													

The power manager contains a 32-bit register that configures the processor sleep wakeup sequence. The PSR, shown in Table 2, provides a single bit called FWAKE which is used to select between the standard and fast sleep wakeup sequences. The PMFW register is reset by a hardware reset,

GPIO reset, watchdog reset, but is not cleared by the sleep wakeup sequence. Using an exception handler to invoke sleep in response to a power fault event is advantageous because software can clear the PMFW[FWAKE] bit and configure the power management IC to use PWR_EN to disable the core power supply during sleep to minimize power consumption from a critically low battery. Also, the PCFR[OPDE] bit must be cleared to enable the 3.6864 MHz oscillator during sleep when fast sleep wakeup is selected by setting the PMFW[FWAKE] bit.

This is a read/write register. Ignore reads from reserved bits. Write zeros to reserved bits.

S3. Voltage for low frequency range raised to 1.0V

Problem: Voltage and frequency range 1, for up to 118 MHz operation, is now specified at 1.0V -5% +10.

Change this entry in Table 5-2 of the *Intel® PXA26x Processor Family Electrical, Mechanical, and Thermal Specification*:

V _{VCC_1}	Voltage applied on VCC, PLL_VCC	0.8075	0.85	0.935	V
--------------------	---------------------------------	--------	------	-------	---

to read

V _{VCC_1}	Voltage applied on VCC, PLL_VCC	0.95	1.00	1.1	V
--------------------	---------------------------------	------	------	-----	---

Status: Fixed

Specification Clarifications

Note: There are no specification clarifications at this time.

Documentation Changes

D1. VLIO nOE/nPWE de-assertion time of RDN+1.

Affected Docs: Intel® PXA26x Processor Family Developer's Manual

Issue: Section 6.8.5 states:

Before a subsequent data beat, nOE or nPWE remains de-asserted for RDN+1 memory cycles.

It should state:

Before a subsequent data beat, nOE or nPWE remains de-asserted for RDN+2 memory cycles.

Status: Doc

D2. VLIO nOE/nPWE de-assertion time of RDN+1 for Figure 6-18 and 6-19.

Affected Docs: Intel® PXA26x Processor Family Developer's Manual

Issue: Figure 6-18 and Figure 6-19 states:

RDN+1

They should state:

RDN+2

Status: Doc

D3. VLIO nOE/nPWE de-assertion time of RDN+1 for Table 6-22.

Affected Docs: Intel® PXA26x Processor Family Developer's Manual

Issue: Table 6-26 states:

MSCx[RTx]	Device Type	Timing (Memory Cycles)					
		Burst Read Address Assert	nOE Assert	Burst nOE Deassert	Burst Write Address Assert	nWE Assert	Burst nWE Deassert
100	Variable latency I/O	RDF+RDN+2+waits	RDF+1+waits	RDN+1	RDF+RDN+2+waits	RDF+1+waits	RDN+1

It should read:

MSCx[RTx]	Device Type	Timing (Memory Cycles)					
		Burst Read Address Assert	nOE Assert	Burst nOE Deassert	Burst Write Address Assert	nWE Assert	Burst nWE Deassert
100	Variable latency I/O	RDF+RDN+2+waits	RDF+1+waits	RDN+2	RDF+RDN+2+waits	RDF+1+waits	RDN+2

Status: Doc

D4. VLIO nOE/nPWE de-assertion time of RDN+1 for Table 6-21.

Affected Docs: Intel® PXA26x Processor Family Developer's Manual

Issue: Table 6-25 (sheet 1 of 3) states:

0X4800 0008/ 0x4800 000C/ 0x4800 0010												MSC0/ MSC1/ MSC2												processor													
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																					
RBUF1/3/5			RRR1/3/5			RDN1/3/5			RDF1/3/5			RBW1/3/5		RT1/3/5		RBUF0/2/4		RRR0/2/4		RDN0/2/4		RDF0/2/4		RBW0/2/4		RT0/2/4											
0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *																																					
Bits			Access			Name			Description																												
11:8			Read/Write			RDNx<3:0>			ROM DELAY NEXT ACCESS: Address to data valid for subsequent access to burst ROM or flash is equal to (RDNx + 1) memclks. nWE assertion for write accesses to SRAM is equal to (RDFx + 1) memclks. The nOE (nPWE) de-assert time between each beat of read/write for variable latency I/O is equal to (RDNx + 1) memclks. For variable latency I/O, this number must be greater than or equal to 2.																												

It should read:

0X4800 0008/ 0x4800 000C/ 0x4800 0010												MSC0/ MSC1/ MSC2												processor													
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																					
RBUF1/3/5			RRR1/3/5			RDN1/3/5			RDF1/3/5			RBW1/3/5		RT1/3/5		RBUF0/2/4		RRR0/2/4			RDN0/2/4			RDF0/2/4			RBW0/2/4		RT0/2/4								
0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *																																					
0			1			1			1			1			1			0			0			0			0			0			0				
Bits			Access			Name			Description																												
11:8			Read/Write			RDNx<3:0>			ROM DELAY NEXT ACCESS: Address to data valid for subsequent access to burst ROM or flash is equal to (RDNx + 1) memclks. nWE assertion for write accesses to SRAM is equal to (RDFx + 1) memclks. The nOE (nPWE) de-assert time between each beat of read/write for variable latency I/O is equal to (RDNx + 2) memclks. For variable latency I/O, this number must be greater than or equal to 2.																												

Status: Doc

D5. Table 3-1: Core PLL Output Frequencies for 3.6864 MHz Crystal

Affected Docs: Intel® PXA26X Processor Developers Manual



Issue: Table values incorrect; changed to reflect those from Table 3-1 in the PXA255 Processor Developers Manual.

Table 3-1. Core PLL Output Frequencies for 3.6864 MHz Crystal (corrected)

L	M	Turbo Mode Frequency (MHz) for Values “N” and Core Clock Configuration Register (CCCR[15:0]) programming for Values of “N”:				PXbus Frequency (MHz)	MEM, LCD Frequency (MHz)	SDRAM max Freq (MHz)
		1.00 (Run)	1.50	2.00	3.00			
27	1	99.5 @1.0 V	—	199.1 @1.0 V	298.6 @1.1 V	50	99.5	99.5
36	1	132.7 @1.0 V	—	—	—	66	132.7	66
27	2	199.1 @1.1 V	298.6 @1.1 V	398.1 @1.3 V	—	99.5	99.5	99.5
36	2	265.4 1.1 V	—	—	—	132.7	132.7	66
45	2	331.8 @1.3 V	—	—	—	165.9	165.9	83
27	4	398.1 @1.3 V	—	—	—	196	99.5	99.5

Status: Doc

D6. Table 12-13: UDC Control Function Register

Affected Docs: Intel® PXA26X Processor Developers Manual

Issue: New register UDCCFR added as section 12.6.2, Table 12-13 and subsections 12.6.2.1 and 12.6.2.2.

12.6.2 UDC Control Function Register (UDCCFR)

The UDC Control Function register (UDCCFR) contains 1 mode bit and 1 enable bit that lets software delay sending back an ACK response to SET_CONFIG or SET_INTERFACE commands from the host. The remaining bits are reserved.

Table 12-13. UDC Control Function Register

0h 4060_0008

UDCCFR

USB Device Controller

Bit	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	Reserved																									AREN	MB1				ACM	MB1			
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1		

Bits	Name	Description
31:8	—	Reserved – Read as unknown and must be written as zero.
7	AREN	ACK RESPONSE ENABLE (read/write 1 to set) 0 = Send NAK response to SET_CONFIGURATION and SET_INTERFACE commands 1 = Send ACK response to SET_CONFIGURATION and SET_INTERFACE commands
6:2	MB1	MB1 This bit must be set to 1. 0 = Reserved 1 = Must be configured to 1.
2	ACM	ACK CONTROL MODE (read/write 1 to set) 0 = Send ACK response to SET_CONFIGURATION and SET_INTERFACE commands with no user intervention (B-step default) 1 = Send NAK response to SET_CONFIGURATION and SET_INTERFACE commands until UDCCFR[AREN] = 1
1	MB1	MB1 This bit must be set to 1. 0 = Reserved 1 = Must be configured to 1.

12.6.2.1 ACK Control Mode

The ACK control mode (ACM) bit enables user control of the ACK response to the status IN requests of SET_CONFIGURATION and SET_INTERFACE commands. When ACM is set to 0, the UDC automatically responds to the STATUS IN request following a SET_CONFIGURATION and SET_INTERFACE with an ACK. When ACM is set to 1, the UDC responds to the STATUS IN request following a SET_CONFIGURATION and SET_INTERFACE command with a NAK until AREN is set to 1. When the user sets AREN to 1, the UDC responds with an ACK to the next STATUS IN request.

12.6.2.2 ACK Response Enable

When ACM = 1, the ACK response enable (AREN) bit enables user control of the ACK response to the status IN requests of SET_CONFIGURATION and SET_INTERFACE commands. When ACM is set to 1, the UDC responds to the STATUS IN request following a

SET_CONFIGURATION and SET_INTERFACE command with a NAK until AREN is set to 1. When the user sets AREN to 1, the UDC responds with an ACK to the next STATUS IN request. AREN is cleared by the UDC when another SETUP command is received.

Status: Doc

D7. Update to Register Table 12-33 at end of Chapter 12.

Affected Docs: Intel® PXA26X Processor Developers Manual

Issue: Table had erroneous entries; revised to reflect correct entries.

Figure 12-33. UDC Control, Data, and Status Register Locations (Sheet 1 of 2)

Address	Name	Description
0h 4060 0000	UDCCR	UDC Control Register
0h 4060 0004	—	Reserved for future use
0h4060_0008	UDCCFR	UDC Control Function Register
0h 4060 000C	—	Reserved for future use
0h 4060 0010	UDCCS0	UDC Endpoint 0 Control/Status Register
0h 4060 0014	UDCCS1	UDC Endpoint 1 (IN) Control/Status Register
0h 4060 0018	UDCCS2	UDC Endpoint 2 (OUT) Control/Status Register
0h 4060 001C	UDCCS3	UDC Endpoint 3 (IN) Control/Status Register
0h 4060 0020	UDCCS4	UDC Endpoint 4 (OUT) Control/Status Register
0h 4060 0024	UDCCS5	UDC Endpoint 5 (Interrupt) Control/Status Register
0h 4060 0028	UDCCS6	UDC Endpoint 6 (IN) Control/Status Register
0h 4060 002C	UDCCS7	UDC Endpoint 7 (OUT) Control/Status Register
0h 4060 0030	UDCCS8	UDC Endpoint 8 (IN) Control/Status Register
0h 4060 0034	UDCCS9	UDC Endpoint 9 (OUT) Control/Status Register
0h 4060 0038	UDCCS10	UDC Endpoint 10 (Interrupt) Control/Status Register
0h 4060 003C	UDCCS11	UDC Endpoint 11 (IN) Control/Status Register
0h 4060 0040	UDCCS12	UDC Endpoint 12 (OUT) Control/Status Register

Table 12-33. UDC Control, Data, and Status Register Locations (Sheet 2 of 2)

Address	Name	Description
0h 4060 0040	UDCCS12	UDC Endpoint 12 (OUT) Control/Status Register
0h 4060 0044	UDCCS13	UDC Endpoint 13 (IN) Control/Status Register
0h 4060 0048	UDCCS14	UDC Endpoint 14 (OUT) Control/Status Register
0h 4060 004C	UDCCS15	UDC Endpoint 15 (Interrupt) Control/Status Register
0h 4060 0050	UICR0	UDC Interrupt Control Register 0
0h 4060 0054	UICR1	UDC Interrupt Control Register 1
0h 4060 0058	USIR0	UDC Status Interrupt Register 0
0h 4060 005C	USIR1	UDC Status Interrupt Register 1

Table 12-33. UDC Control, Data, and Status Register Locations (Sheet 2 of 2)

0h 4060 0060	UFNHR	UDC Frame Number Register High
0h 4060 0064	UFNLR	UDC Frame Number Register Low
0h 4060 0068	UBCR2	UDC Byte Count Register 2
0h 4060 006C	UBCR4	UDC Byte Count Register 4
0h 4060 0070	UBCR7	UDC Byte Count Register 7
0h 4060 0074	UBCR9	UDC Byte Count Register 9
0h 4060 0078	UBCR12	UDC Byte Count Register 12
0h 4060 007C	UBCR14	UDC Byte Count Register 14
0h 4060 0080	UDDR0	UDC Endpoint 0 Data Register
0h 4060 0100	UDDR1	UDC Endpoint 1 Data Register
0h 4060 0180	UDDR2	UDC Endpoint 2 Data Register
0h 4060 0200	UDDR3	UDC Endpoint 3 Data Register
0h 4060 0400	UDDR4	UDC Endpoint 4 Data Register
0h 4060 00A0	UDDR5	UDC Endpoint 5 Data Register
0h 4060 0600	UDDR6	UDC Endpoint 6 Data Register
0h 4060 0680	UDDR7	UDC Endpoint 7 Data Register
0h 4060 0700	UDDR8	UDC Endpoint 8 Data Register
0h 4060 0900	UDDR9	UDC Endpoint 9 Data Register
0h 4060 00C0	UDDR10	UDC Endpoint 10 Data Register
0h 4060 0B00	UDDR11	UDC Endpoint 11 Data Register
0h 4060 0B80	UDDR12	UDC Endpoint 12 Data Register
0h 4060 0C00	UDDR13	UDC Endpoint 13 Data Register
0h 4060 0E00	UDDR14	UDC Endpoint 14 Data Register
0h 4060 00E0	UDDR15	UDC Endpoint 15 Data Register

Status: Doc

D8. Update to Table 2-8 at end of Chapter 2 System Architecture

Affected Docs: Intel® PXA26X Processor Developers Manual

Issue: Table had erroneous entries; revised to reflect correct entries.

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 1 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
Memory Controller Pins				
MA[25:0]	OCZ	MEMORY ADDRESS BUS (output): Signals the address requested for memory accesses.	Driven Low	Driven Low
MD[15:0]	ICOCZ	MEMORY DATA BUS (input/output): Lower 16 bits of the data bus.	Hi-Z	Driven Low
MD[31:16]	ICOCZ	MEMORY DATA BUS (input/output): Used for 32-bit memories.	Hi-Z	Driven Low

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 2 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
nOE	OCZ	MEMORY OUTPUT ENABLE (output): Connect to the output enables of memory devices to control data bus drivers.	Driven High	Note [4]
nWE	OCZ	MEMORY WRITE ENABLE (output): Connect to the write enables of memory devices.	Driven High	Note [4]
nSDCS[0]	OCZ	SDRAM CS FOR BANKS 0 THROUGH 3 (output): Connect to the chip select (CS) pins for SDRAM. For the PXA26x processor nSDCS0 can be Hi-Z, nSDCS1-3 cannot.	Driven High	Driven High
nSDCS[1]	OC		Driven High	Driven High
nSDCS[2]/ GPIO[86]	ICOC		Driven High (but see Note[8])	Driven High (but see Note [8])
nSDCS[3]/ GPIO[87]	ICOC		Driven High (but see Note[8])	Driven High (but see Note [8])
DQM[3:0]	OCZ	SDRAM DQM FOR DATA BYTES 3 THROUGH 0 (output): Connect to the data output mask enables (DQM) for SDRAM.	Driven Low	Driven Low
nSDRAS	OCZ	SDRAM RAS (output): Connect to the row address strobe (RAS) pins for all banks of SDRAM.	Driven High	Driven High
nSDCAS	OCZ	SDRAM CAS (output): Connect to the column address strobe (CAS) pins for all banks of SDRAM.	Driven High	Driven High
SDCKE[0]	OC	Synchronous Static Memory clock enable (output): Connect to the CKE pins of SMROM. The memory controller provides control register bits for deassertion.	Driven Low	Driven Low
SDCKE[1]	OC	SDRAM OR SYNCHRONOUS STATIC MEMORY CLOCK ENABLE (output): Connect to the clock enable pins of SDRAM. It is deasserted during sleep. SDCKE[1] is always deasserted upon reset. The memory controller provides control register bits for deassertion.	Driven Low	Driven Low
SDCLK[0]	OC	SYNCHRONOUS STATIC MEMORY CLOCK (output): Connect to the clock (CLK) pins of SMROM. It is driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[0] control register assertion bit defaults to on if the boot-time static memory bank 0 is configured for SMROM.		
SDCLK[1]	OCZ	SDRAM CLOCKS (output): Connect SDCLK[1] and SDCLK[2] to the clock pins of SDRAM in bank pairs 0/1 and 2/3, respectively. They are driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[2:1] control register assertion bits are always deasserted upon reset.	Driven Low	Driven Low
SDCLK[2]	OC		Driven Low	Driven Low

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 3 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
nCS[5]/ GPIO[33]	ICOCZ	STATIC CHIP SELECTS (output): Chip selects to static memory devices such as ROM and flash. Individually programmable in the memory configuration registers. nCS[5:0] can be used with variable latency I/O devices.	Pulled High Note [1]	Note [4]
nCS[4]/ GPIO[80]	ICOCZ			
nCS[3]/ GPIO[79]	ICOCZ			
nCS[2]/ GPIO[78]	ICOCZ			
nCS[1]/ GPIO[15]	ICOCZ			
nCS[0]	ICOCZ	STATIC CHIP SELECT 0 (output): Chip select for the boot memory. nCS[0] is a dedicated pin used for internal flash.	Driven High	Note [4]
RD/nWR/ GPIO[88]	OCZ	READ/WRITE FOR STATIC INTERFACE (output): Signals that the current transaction is a read or write.	Driven Low (but see Note[8])	Driven High (but see Note[8])
RDY/ GPIO[18]	ICOCZ	VARIABLE LATENCY I/O READY PIN (input): Notifies the memory controller when an external bus device is ready to transfer data.	Pulled High Note [1]	Note [3]
L_DD[8]/ GPIO[66]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. Memory Controller alternate bus master request. (input) Allows an external device to request the system bus from the Memory Controller.	Pulled High Note [1]	Note [3]
L_DD[15]/ GPIO[73]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. Memory Controller grant. (output) Notifies an external device that it has been granted the system bus.	Pulled High Note [1]	Note [3]
MBGNT/GP[13]	ICOCZ	MEMORY CONTROLLER GRANT (output): Notifies an external device that it has been granted the system bus.	Pulled High Note [1]	Note [3]
MBREQ/GP[14]	ICOCZ	MEMORY CONTROLLER ALTERNATE BUS MASTER REQUEST (input): Allows an external device to request the system bus from the Memory Controller.	Pulled High Note [1]	Note [3]
PCMCIA/CF Control Pins				
nPOE/ GPIO[48]	ICOCZ	PCMCIA OUTPUT ENABLE (output): Reads from PCMCIA memory and to PCMCIA attribute space.	Pulled High Note [1]	Note [5]
nPWE/ GPIO[49]	ICOCZ	PCMCIA WRITE ENABLE (output): Performs writes to PCMCIA memory and to PCMCIA attribute space. Also used as the write enable signal for Variable Latency I/O.	Pulled High Note [1]	Note [5]
nPIOW/ GPIO[51]	ICOCZ	PCMCIA I/O WRITE (output): Performs write transactions to PCMCIA I/O space.	Pulled High Note [1]	Note [5]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 4 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
nPIOR/ GPIO[50]	ICOCZ	PCMCIA I/O READ (output): Performs read transactions from PCMCIA I/O space.	Pulled High Note [1]	Note [5]
nPCE[2]/ GPIO[53]	ICOCZ	PCMCIA CARD ENABLE 2 (output): Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane. MMC clock. (output) Clock signal for the MMC Controller.	Pulled High Note [1]	Note [5]
nPCE[1]/ GPIO[52]	ICOCZ	PCMCIA CARD ENABLE 1 (outputs): Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane.	Pulled High Note [1]	Note [5]
nIOIS16/ GPIO[57]	ICOCZ	IO SELECT 16 (input): Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.	Pulled High Note [1]	Note [5]
nPWAIT/ GPIO[56]	ICOCZ	PCMCIA WAIT (input): Driven low by the PCMCIA card to extend the length of the transfers to/from the PXA26x processor.	Pulled High Note [1]	Note [5]
PSKTSEL/ GPIO[54]	ICOCZ	PCMCIA SOCKET SELECT (output): Used by external steering logic to route control, address, and data signals to one of the two PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. Has the same timing as the address bus.	Pulled High Note [1]	Note [5]
nPREG/ GPIO[55]	ICOCZ	PCMCIA REGISTER SELECT (output): Indicates that the target address on a memory transaction is attribute space. Has the same timing as the address bus.	Pulled High Note [1]	Note [5]
LCD Controller Pins				
L_DD(7:0)/ GPIO[65:58]	ICOCZ	LCD DISPLAY DATA (outputs): Transfers pixel information from the LCD Controller to the external LCD panel.	Pulled High Note [1]	Note [3]
L_DD[8]/ GPIO[66]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. Memory Controller alternate bus master request. (input) Allows an external device to request the system bus from the Memory Controller.	Pulled High Note [1]	Note [3]
L_DD[9]/ GPIO[67]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC chip select 0. (output) Chip select 0 for the MMC Controller.	Pulled High Note [1]	Note [3]
L_DD[10]/ GPIO[68]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC chip select 1. (output) Chip select 1 for the MMC Controller.	Pulled High Note [1]	Note [3]
L_DD[11]/ GPIO[69]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC clock. (output) Clock for the MMC Controller.	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 5 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
L_DD[12]/ GPIO[70]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. RTC clock. (output) Real time clock 1 Hz tick.	Pulled High Note [1]	Note [3]
L_DD[13]/ GPIO[71]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. 3.6864-MHz clock. (output) Output from 3.6864-MHz oscillator.	Pulled High Note [1]	Note [3]
L_DD[14]/ GPIO[72]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. 32-KHz clock. (output) Output from the 32-KHz oscillator.	Pulled High Note [1]	Note [3]
L_DD[15]/ GPIO[73]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. Memory Controller grant. (output) Notifies an external device it has been granted the system bus.	Pulled High Note [1]	Note [3]
L_FCLK/ GPIO[74]	ICOCZ	LCD FRAME CLOCK (output): Indicates the start of a new frame. Also referred to as Vsync.	Pulled High Note [1]	Note [3]
L_LCLK/ GPIO[75]	ICOCZ	LCD LINE CLOCK (output): Indicates the start of a new line. Also referred to as Hsync.	Pulled High Note [1]	Note [3]
L_PCLK/ GPIO[76]	ICOCZ	LCD PIXEL CLOCK (output): Clocks valid pixel data into the LCD's line shift buffer.	Pulled High Note [1]	Note [3]
L_BIAS/ GPIO[77]	ICOCZ	AC BIAS DRIVE (output): Notifies the panel to change the polarity for some passive LCD panel. For TFT panels, this signal indicates valid pixel data.	Pulled High Note [1]	Note [3]
Full Function UART Pins				
FFRXD/ GPIO[34]	ICOCZ	FULL FUNCTION UART RECEIVE (input): MMC chip select 0. (output) Chip select 0 for the MMC Controller.	Pulled High Note [1]	Note [3]
FFTXD/ GPIO[39]	ICOCZ	FULL FUNCTION UART TRANSMIT (output): MMC chip select 1. (output) Chip select 1 for the MMC Controller.	Pulled High Note [1]	Note [3]
FFCTS/ GPIO[35]	ICOCZ	FULL FUNCTION UART CLEAR-TO-SEND (input)	Pulled High Note [1]	Note [3]
FFDCD/ GPIO[36]	ICOCZ	FULL FUNCTION UART DATA-CARRIER-DETECT (input)	Pulled High Note [1]	Note [3]
FFDSR/ GPIO[37]	ICOCZ	FULL FUNCTION UART DATA-SET-READY (input)	Pulled High Note [1]	Note [3]
FFRI/ GPIO[38]	ICOCZ	FULL FUNCTION UART RING INDICATOR (input)	Pulled High Note [1]	Note [3]
FFDTR/ GPIO[40]	ICOCZ	FULL FUNCTION UART DATA-TERMINAL-READY (output)	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 6 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
FFRTS/ GPIO[41]	ICOCZ	FULL FUNCTION UART REQUEST-TO-SEND (output):	Pulled High Note [1]	Note [3]
Bluetooth UART Pins				
BTRXD/ GPIO[42]	ICOCZ	BLUETOOTH UART RECEIVE (input):	Pulled High Note [1]	Note [3]
BTTXD/ GPIO[43]	ICOCZ	BLUETOOTH UART TRANSMIT (output):	Pulled High Note [1]	Note [3]
BTCTS/ GPIO[44]	ICOCZ	BLUETOOTH UART CLEAR-TO-SEND (input):	Pulled High Note [1]	Note [3]
BTRTS/ GPIO[45]	ICOCZ	BLUETOOTH UART DATA-TERMINAL-READY (output):	Pulled High Note [1]	Note [3]
Standard UART and ICP Pins				
IRRXD/ GPIO[46]	ICOCZ	IRDA RECEIVE SIGNAL (input): Receive pin for the FIR function. STANDARD UART RECEIVE (input)	Pulled High Note [1]	Note [3]
IRTXD/ GPIO[47]	ICOCZ	IRDA TRANSMIT SIGNAL (output): Transmit pin for the Standard UART, SIR and FIR functions. STANDARD UART TRANSMIT (output)	Pulled High Note [1]	Note [3]
MMC Controller Pins				
MMCMD	ICOCZ	MULTIMEDIA CARD COMMAND (bidirectional)	Hi-Z	Hi-Z
MMDAT	ICOCZ	MULTIMEDIA CARD DATA (bidirectional)	Hi-Z	Hi-Z
nPCE[2]/ GPIO[53]	ICOCZ	PCMCIA CARD ENABLE 2 (outputs): Selects a PCMCIA card. Bit one enables the high byte lane and bit zero enables the low byte lane. MMC clock. (output) Clock signal for the MMC Controller.	Pulled High Note [1]	Note [5]
L_DD[9]/ GPIO[67]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC CHIP SELECT 0 (output): Chip select 0 for the MMC Controller.	Pulled High Note [1]	Note [3]
L_DD[10]/ GPIO[68]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC CHIP SELECT 1 (output): Chip select 1 for the MMC Controller.	Pulled High Note [1]	Note [3]
L_DD[11]/ GPIO[69]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. MMC CLOCK (output): Clock for the MMC Controller.	Pulled High Note [1]	Note [3]
FFRXD/ GPIO[34]	ICOCZ	FULL FUNCTION UART RECEIVE (input) MMC CHIP SELECT 0 (output): Chip select 0 for the MMC Controller.	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 7 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
FFTXD/ GPIO[39]	ICOCZ	FULL FUNCTION UART TRANSMIT (output) MMC CHIP SELECT 1 (output): Chip select 1 for the MMC Controller.	Pulled High Note [1]	Note [3]
MMCLK/GP[6]	ICOCZ	MMC CLOCK (output): Clock signal for the MMC Controller.	Pulled High Note [1]	Note [3]
MMCS0/GP[8]	ICOCZ	MMC CHIP SELECT 0 (output): Chip select 0 for the MMC Controller.	Pulled High Note [1]	Note [3]
MMCS1/GP[9]	ICOCZ	MMC CHIP SELECT 1 (output): Chip select 1 for the MMC Controller.	Pulled High Note [1]	Note [3]
SSP Pins				
SSPCLK/ GPIO[23]	ICOCZ	SYNCHRONOUS SERIAL PORT CLOCK (output)	Pulled High Note [1]	Note [3]
SSPSFRM/ GPIO[24]	ICOCZ	SYNCHRONOUS SERIAL PORT FRAME (output)	Pulled High Note [1]	Note [3]
SSPTXD/ GPIO[25]	ICOCZ	SYNCHRONOUS SERIAL PORT TRANSMIT (output)	Pulled High Note [1]	Note [3]
SSPRXD/ GPIO[26]	ICOCZ	SYNCHRONOUS SERIAL PORT RECEIVE (input)	Pulled High Note [1]	Note [3]
SSPEXTCLK/ GPIO[27]	ICOCZ	SYNCHRONOUS SERIAL PORT EXTERNAL CLOCK (input)	Pulled High Note [1]	Note [3]
USB Client Pins				
USB_P	IAOAZ	USB CLIENT POSITIVE (bidirectional)	Hi-Z	Hi-Z
USB_N	IAOAZ	USB CLIENT NEGATIVE PIN (bidirectional)	Hi-Z	Hi-Z
Single Ended USB Pins				
USB_RCV/ GPIO[9]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE RCV (input): Differential receive data from the USB transceiver.	Pulled High Note [1]	Note [3]
USB_VP/ GPIO[32]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE VP (input): Gated version of D+ from the USB transceiver.	Pulled High Note [1]	Note [3]
USB_VM/ GPIO[34]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE VM (input): Gated version of D- from the USB transceiver.	Pulled High Note [1]	Note [3]
USB_VPO/ GPIO[39]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE VPO (output): Output to USB transceiver differential driver D+.	Pulled High Note [1]	Note [3]
USB_VMO/ GPIO[56]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE VMO (output): Output to USB transceiver differential driver D-.	Pulled High Note [1]	Note [3]
USB_nOE/ GPIO[57]	ICOCZ	USB CLIENT SINGLE-ENDED INTERFACE nOE (output): Output enable for the USB transceiver to transmit data on the bus. When deasserted, the transceiver is in receive mode.	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 8 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
AC97 Controller and I2S Controller Pins				
BITCLK/ GPIO[28]	ICOCZ	AC97 AUDIO PORT BIT CLOCK (input): AC97 clock is generated by Codec 0 and fed into the PXA26x processor and Codec 1. AC97 AUDIO PORT BIT CLOCK (output): AC97 clock is generated by the PXA26x processor. I2S BIT CLOCK (input): I2S clock is generated externally and fed into PXA26x processor. I2S BIT CLOCK (output): I2S clock is generated by the PXA26x processor.	Pulled High Note [1]	Note [3]
SDATA_IN0/ GPIO[29]	ICOCZ	AC97 AUDIO PORT DATA IN (input): Input line for Codec 0. I2S DATA IN (input): Input line for the I2S Controller.	Pulled High Note [1]	Note [3]
SDATA_IN1/ GPIO[32]	ICOCZ	AC97 AUDIO PORT DATA IN (input): Input line for Codec 1. I2S SYSTEM CLOCK (output): System clock from I2S Controller.	Pulled High Note [1]	Note [3]
SDATA_OUT/ GPIO[30]	ICOCZ	AC97 AUDIO PORT DATA OUT (output): Output from the PXA26x processor to Codecs 0 and 1. I2S DATA OUT (output): Output line for the I2S Controller.	Pulled High Note [1]	Note [3]
SYNC/ GPIO[31]	ICOCZ	AC97 AUDIO PORT SYNC SIGNAL (output): Frame sync signal for the AC97 Controller. I2S SYNC (output): Frame sync signal for the I2S Controller.	Pulled High Note [1]	Note [3]
nACRESET/ GPIO[89]	ICOC	AC97 AUDIO PORT RESET SIGNAL (output)	Driven Low (but see Note[8])	Driven Low (but see Note[8])
I2C Controller Pins				
SCL	ICOCZ	I2C CLOCK (bidirectional)	Hi-Z	Hi-Z
SDA	ICOCZ	I2C DATA (bidirectional).	Hi-Z	Hi-Z
PWM Pins				
PWM[1:0]/ GPIO[17:16]	ICOCZ	PULSE WIDTH MODULATION CHANNELS 0 AND 1 (outputs)	Pulled High Note [1]	Note [3]
DMA Pins				
DREQ[1:0]/ GPIO[19:20]	ICOCZ	DMA REQUEST (input): Notifies the DMA Controller that an external device requires a DMA transaction. DREQ[1] is GPIO[19]. DREQ[0] is GPIO[20].	Pulled High Note [1]	Note [3]
GPIO Pins				
GPIO[1:0]	ICOCZ	GENERAL PURPOSE I/O: Walk-up sources on both rising and falling edges on nRESET.	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 9 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
GPIO[14:2]	ICOCZ	GENERAL PURPOSE I/O: More wake-up sources for sleep mode.	Pulled High Note [1]	Note [3]
GPIO[22:21]	ICOCZ	GENERAL PURPOSE I/O: Additional General Purpose I/O pins.	Pulled High Note [1]	Note [3]
GPIO[85]	ICOCZ	GENERAL PURPOSE I/O: Additional General Purpose I/O pins.	Pulled High Note [1]	Note [3]
Crystal and Clock Pins				
PXTAL	OA	3.6864-MHz CRYSTAL OUTPUT: No external caps are required.	Note [2]	Note [2]
PEXTAL	IA	3.6864-MHz CRYSTAL INPUT: No external caps are required.	Note [2]	Note [2]
TXTAL	OA	32.768-KHz CRYSTAL OUTPUT: No external caps are required.	Note [2]	Note [2]
TEXTAL	IA	32.768-KHz CRYSTAL INPUT: No external caps are required.	Note [2]	Note [2]
L_DD[12]/ GPIO[70]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. RTC CLOCK (output): Real time clock 1 Hz tick.	Pulled High Note [1]	Note [3]
L_DD[13]/ GPIO[71]	ICOCZ	LCD DISPLAY DATA (output): Transfers the pixel information from the LCD Controller to the external LCD panel. 3.6864-MHz CLOCK (output): Output from 3.6864-MHz oscillator.	Pulled High Note [1]	Note [3]
L_DD[14]/ GPIO[72]	ICOCZ	LCD DISPLAY DATA (output): Transfers pixel information from the LCD Controller to the external LCD panel. 32-KHz CLOCK (output): Output from the 32-KHz oscillator.	Pulled High Note [1]	Note [3]
48MHz/GP[7]	ICOCZ	48-MHz CLOCK (output): Peripheral clock output derived from the PLL. NOTE: This clock is only generated when the USB unit clock enable is set.	Pulled High Note [1]	Note [3]
RTCCLK/GP[10]	ICOCZ	REAL TIME CLOCK (output): 1-Hz output derived from the 32-KHz or 3.6864-MHz output.	Pulled High Note [1]	Note [3]
3.6MHz/GP[11]	ICOCZ	3.6864-MHz CLOCK (output): Output from 3.6864-MHz oscillator.	Pulled High Note [1]	Note [3]
32KHz/GP[12]	ICOCZ	32-KHz CLOCK (output): Output from the 32-KHz oscillator.	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 10 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
Miscellaneous Pins				
BOOT_SEL [2:0]	IC	BOOT SELECT PINS (input): Indicates type of boot device. See Section 18.1, "Initialization" for information on configuring BOOT_SEL for proper flash initialization.	Input	Input
PWR_EN	OC	POWER ENABLE FOR THE POWER SUPPLY (output): When negated, it signals the power supply to remove power to the core because the system is entering sleep mode.	Driven High	Driven low while entering sleep mode. Driven high when sleep exit sequence begins.
nBATT_FAULT	IC	MAIN BATTERY FAULT (input): Signals that main battery is low or removed. Assertion causes PXA26x processor to enter sleep mode or force an imprecise data exception, which cannot be masked. PXA26x processor will not recognize a wake-up event while this signal is asserted. Minimum assertion time for nBATT_FAULT is 1 ms.	Input	Input
nVDD_FAULT	IC	VDD FAULT (input): Signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA26x processor to enter sleep mode or force an Imprecise Data Exception, which cannot be masked. nVDD_FAULT is ignored after a wake-up event until the power supply timer completes (approximately 10 ms). Minimum assertion time for nVDD_FAULT is 1 ms.	Input	Input
nRESET	IC	HARD RESET (input): Level sensitive input used to start the processor from a known address. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable.	Input	Input. Driving low during sleep will cause normal reset sequence and exit from sleep mode.
nRESET_OUT	OC	RESET OUT (output): Asserted when nRESET is asserted and deasserts after nRESET is deasserted but before the first instruction fetch. nRESET_OUT is also asserted for "soft" reset events: sleep, watchdog reset, or GPIO reset.	Driven low during any reset sequence – driven high prior to first fetch.	Driven Low
JTAG and Test Pins				
nTRST	IC	JTAG TEST INTERFACE RESET: Resets the JTAG/Debug port. If JTAG/Debug is used, drive nTRST from low to high either before or at the same time as nRESET. If JTAG is not used, nTRST must be either tied to nRESET or tied low.	Input	Input
TDI	IC	JTAG TEST DATA INPUT (input): Data from the JTAG controller is sent to the PXA26x processor using this pin. This pin has an internal pull-up resistor.	Input	Input
TDO	OCZ	JTAG TEST DATA OUTPUT (output): Data from the PXA26x processor is returned to the JTAG controller using this pin.	Hi-Z	Hi-Z

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 11 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
TMS	IC	JTAG TEST MODE SELECT (input): Selects the test mode required from the JTAG controller. This pin has an internal pull-up resistor.	Input	Input
TCK	IC	JTAG TEST CLOCK (input): Clock for all transfers on the JTAG test interface.	Input	Input
TEST	IC	TEST MODE (input): Reserved. Must be grounded.	Input	Input
TESTCLK	IC	TEST CLOCK (input): Reserved. Must be grounded.	Input	Input
Power and Ground Pins				
VCC	SUP	INTERNAL LOGIC POSITIVE SUPPLY: Must be connected to the low voltage (.85 – 1.3v) supply on the PCB.	Powered	Note [6]
VSS	SUP	INTERNAL LOGIC GROUND SUPPLY: Must be connected to the common ground plane on the PCB.	Grounded	Grounded
PLL_VCC	SUP	PLLS AND OSCILLATORS POSITIVE SUPPLY: Must be connected to the common low voltage supply.	Powered	Note [6]
PLL_VSS	SUP	PLL GROUND SUPPLY: Must be connected to common ground plane on the PCB.	Grounded	Grounded
VCCQ	SUP	CMOS I/O POSITIVE SUPPLY: EXCEPT memory bus and PCMCIA pins. Must be connected to the common 2.775 – 3.3v supply on the PCB.	Powered	Note [7]
VSSQ	SUP	CMOS I/O GROUND SUPPLY: Except memory bus and PCMCIA pins. Must be connected to the common ground plane on the PCB.	Grounded	Grounded
VCCN	SUP	MEMORY BUS AND PCMCIA PINS POSITIVE SUPPLY: Must be connected to the common 2.5 – 3.3v supply on the PCB.	Powered	Note [7]
VSSN	SUP	MEMORY BUS AND PCMCIA PINS GROUND SUPPLY: Must be connected to the common ground plane on the PCB.	Grounded	Grounded
Network SSP pins				
NSSPCLK/ GPIO[81]	ICOCZ	NETWORK SYNCHRONOUS SERIAL PORT CLOCK	Pulled High Note [1]	Note [3]
NSSPSFRM/ GPIO[82]	ICOCZ	NETWORK SYNCHRONOUS SERIAL PORT FRAME SIGNAL	Pulled High Note [1]	Note [3]
NSSPTXD/ GPIO[83]	ICOCZ	NETWORK SYNCHRONOUS SERIAL PORT TRANSMIT	Pulled High Note [1]	Note [3]
NSSPRXD/ GPIO[84]	ICOCZ	NETWORK SYNCHRONOUS SERIAL PORT RECEIVE	Pulled High Note [1]	Note [3]
Audio SSP Pins				
ASSPCLK/ GPIO[28]	ICOCZ	AUDIO SYNCHRONOUS SERIAL PORT CLOCK	Pulled High Note [1]	Note [3]

Table 2-8. Pin and Signal Descriptions for the PXA26x Processor Family (Sheet 12 of 12)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
ASSPSFRM/ GPIO[31]	ICOCZ	AUDIO SYNCHRONOUS SERIAL PORT FRAME SIGNAL	Pulled High Note [1]	Note [3]
ASSPTXD/ GPIO[30]	ICOCZ	AUDIO SYNCHRONOUS SERIAL PORT TRANSMIT	Pulled High Note [1]	Note [3]
ASSPRXD/ GPIO[29]	ICOCZ	AUDIO SYNCHRONOUS SERIAL PORT RECEIVE	Pulled High Note [1]	Note [3]
HWUART Pins				
HWTXD/ GPIO[48]	ICOCZ	HARDWARE UART TRANSMIT DATA	Pulled High Note [1]	Note [3]
HWRXD/ GPIO[49]	ICOCZ	HARDWARE UART RECEIVE DATA	Pulled High Note [1]	Note [3]
HWCTS/ GPIO[50]	ICOCZ	HARDWARE UART CLEAR-TO-SEND	Pulled High Note [1]	Note [3]
HWRTS/ GPIO[51]	ICOCZ	HARDWARE UART REQUEST-TO-SEND	Pulled High Note [1]	Note [3]
Internal flash pins (See Section 18, "Internal Flash" for more information)				
nRST_F	IC	RESET FOR FLASH ONLY (input): Resets internal circuitry and inhibits all operations. Exit from reset places flash in asynchronous read-array mode.	—	—
nWP_F	IC	FLASH WRITE PROTECT (input): Enables the lock-down mechanism. Blocks locked down cannot be unlocked with the unlock command. nWP_F high overrides the lock-down function enabling blocks to be erased or programmed through software.	—	—
VPEN_F	IC	FLASH ERASE/PROGRAM/BLOCK LOCK ENABLE (input): Controls device protection. When VPEN_F is less than the lock voltage, flash contents are protected against Program and Erase.	—	—
WAIT_F1	OCZ	FLASH WAIT (output): Indicates invalid data in synchronous-read (burst) modes. Not used by the processor, can be used for flash memory programmers.	—	—
WAIT_F2				
VCC_F	SUP	FLASH CORE LOGIC SUPPLY: Writes to the flash array are inhibited when VCC_F is less than lockout voltage. Operations at invalid VCC voltages must not be attempted.	—	—
VSS_F	SUP	FLASH CORE GROUND: Ground reference for flash core.	—	—
VCCQ_F	SUP	FLASH I/O POWER SUPPLY: Must be the same voltage as the PXA26x processor VCCN.	—	—
VSSQ_F	SUP	FLASH I/O GROUND: Ground reference for flash I/O.	—	—

Status: Doc

§§



